The Impact of Soft Error On C-Element with Different Technology

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***Abstract*—This paper presents current injection resemble single event upset (SEU) current at the vulnerable nodes on C-elements in particular Single Inverter with Inverter Latch (SIL) under two different technology 90nm and 180nm. C-element mainly uses in asynchronous circuits as the demand of consuming low power continue to become more important compared with synchronous circuits. However, one of the problems of asynchronous circuits is that they stay sensitive to SEU continuously for the whole cycle of operation. For asynchronous circuits, an acknowledgement signal is sent to the preceding register after the current operation is finished, indicating it is ready for the next operation. In the event of SEU hitting one of the registers, no acknowledgement signal is sent and therefore the preceding register does not assign the next operation to the current computational block. It is observed that the size of the transistor is the most important factors of critical charge variation since it has the highest standard deviation compared with temperature. This is due to the increasing the size of the transistors increases the gate capacitance from the output and therefore the collected charge needed to flip the output is also larger. However, as the size of the circuit is bigger, the probability of hitting by SEU is also increased even though the circuit is more resistant against SEU. The least significant factor is the temperature. As the temperature increased, the mobility of the carrier is reduced and degrades the performance of the transistor.**

***Index Terms*—C-Element; Pipelining; Asynchronous Circuit; Low Power.**

I. INTRODUCTION

Soft error which caused Single event upset (SEU) is defined as "Radiation-induced errors in microelectronic circuits caused when charged particles (usually from the radiation belts or from cosmic rays) lose energy by ionizing the medium through which they pass, leaving behind a wake of electron-hole pairs" [1]. SEU has been identified as a possible cause of data corruption. The term 'soft error' refers to a temporary error that occurs as a result of particles (alpha particles from packaging or neutrons from the atmosphere) striking the silicon structures and causing the state to change from high to low or from low to high. This electrical effect happens due to the generated electron-hole pairs in the reverse-biased junction of the victim device. The drain of an off PMOS and drain of an off NMOS transistor are more vulnerable toward soft error. Figure 1 shows the single event transient (SET) produced [2]. A neutron from the atmosphere strikes the silicon causing a collision between the nucleus and the neutron within the substrate. The density of electron-hole pairs is produced by particles, as shown in Figure 1(a). The carriers are swept to diffusion junction by an electric field and cause the charge collection to expand due to drift current (Figure 1(b)), resulting in the sudden current pulse. Then, the diffusion current dominates until all the excess carriers have been removed from the junction area (Figure 1(c)). The size of the funnel, as shown in Figure 1(b), and collecting time are very much inversely proportional to the substrate doping. The collection time is usually completed within picoseconds and the diffusion current begins to dominate until all the excess carriers have been collected [3].The study of soft error in 6T SRAM involving 90nm and 180 technology by [4] focused the sensitive nodes in the SRAM

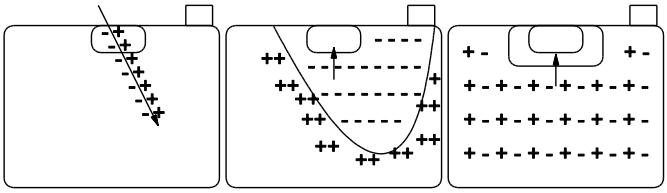

Figure 1: SEU produced

Asynchronous circuit is getting popular due to the non-global clock used in the system.The implementation of an asynchronous circuit by employing a buffer which acts as a latch is shown in Figure 2. Combinational logics are inserted between buffers. The completion detector (CD) is used to generate an acknowledgement signal for the preceding buffers to indicate that the current buffers are ready to process new data. Despite all the advantages of asynchronous circuits, mainly on low power, asynchronous circuits have two major weakness: deadlock and complexity of the design. Deadlock refers to a situation where the system fails to proceed to the next stage due to two or more processes expecting a response from each other and blocking each other from continuing. It is a common situation in asynchronous design that the system faces deadlock due to incorrect circuit design, token mismatch and also arbitration. Single event upset (SEU) can also cause a circuit to have deadlock due to data corruption. Nowadays, the dimensions of transistors are very small, as the technology nodes of 90nm and below. The drain current and the threshold voltage are reduced with voltage scaling. As a result, radiation-induced soft errors in the combinational logic are gaining increasing attention and are expected to become as important as directly induced errors for state elements. Asynchronous buffers are made by cascading C-elements, as shown in Figure 3. The first port of a C-element is reserved for the data and the second port is for the acknowledgement signal. A C-element is used as it is capable of holding data and controlling data independently. Like any other memory element, using a C-element as a buffer is subject to SEU error. The corrupted output is generated when one of the nodes in the C-element suffers SEU error.

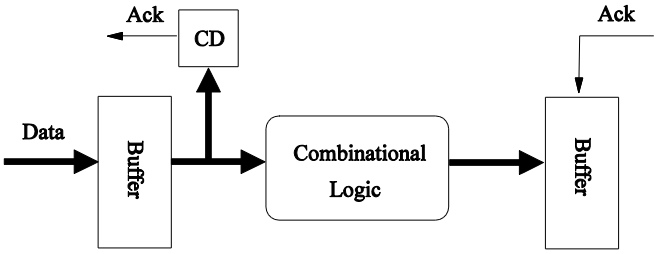

Figure 2: Asynchronous implementation

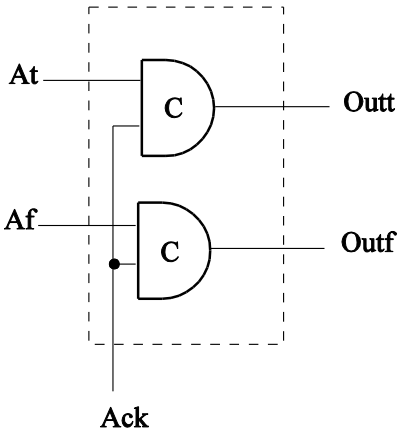

Figure 3: Asynchronous buffer implementation

II. METHODOLOGY OF THE EXPERIMENTS

A current pulse is modelled as current to cause Single Event Upset. It can be represented as having fast rising time and slow falling time. The amplitude, rising time and falling time of the current pulse depend on factors such as the type of particle, the energy of the particle and the angle of the strike. These factors can add complexities to modelling current pulse. The model shown in Figure 4 is used as a current injection to compare the critical charges between the nodes and C-elements. The model is based on [5] with the rising and falling times of current pulse to be 50 ps and 164 ps respectively and 10 ps for the pulse width (Time) [6,7]. The peak current is a variable.

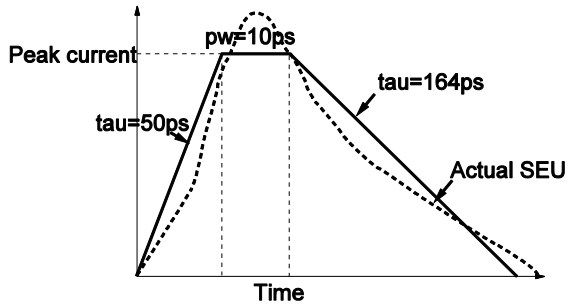

Figure 4: SEU Current Modelling

In order to compare different technology against SEU, the circuits chosen are Single Rail with Inverter Latch (SIL) C-Element as shown by Figure 5(a) and the corresponding layout Figure 5(b). The circuit is modelled to have the same width of the main transistors and the feedback transistors. For this purpose, two different technology of Cadence is used in the simulation: UMC90nm and 180 nm.

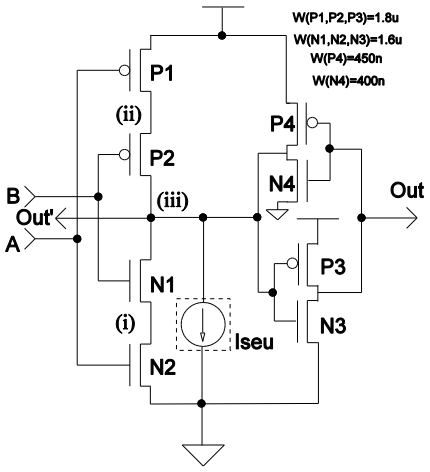

Figure 5(a): SIL Configuration [8]

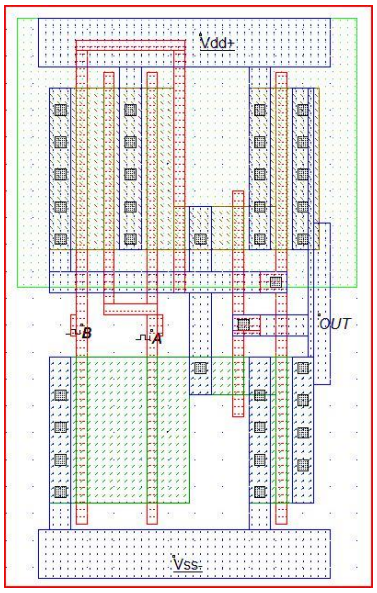

Figure 5(b): Layout SIL Configuration

A SIL circuit consists of main pull up transistors (P1, P2), main pull-down transistors (N1, N2), inverter (P3, N3) and weak inverter (P4, N4). For UMC 90 nm, the total area corresponding to SIL configuration is 18.2 μm^2 and 72.6 μm^2 for 180 nm. The feedback is weaker so that it can be overpowered by the main pull up and pull-down transistors. Suppose both inputs *A* and *B* are low causing the main pull up transistors to change the output *Out* to low. Similarly, if both inputs *A* and *B* are high causing the main pull-down transistors to change the output *Out* to high. If the inputs are not equal, transistors P1 and P2 are disconnected from the power supply and transistors N1 and N2 are disconnected from the ground. The state of output *Out* is maintained by feedback inverters. The vulnerable Nodes are identified. The current pulses are injected at the main transistors and the output of the circuit is shown in Figure 5(a).

The sources of variations in the analysis are the size of transistor (technology) and temperature. It is assumed these parameters are Gaussian and mutually independent. The steps of experiments are the following:

i. The Set inputs A=1, B=0. Repeat A=0, B=1. Assuming two inputs are A and B. There is two possibilities combination of input: A=1, B=0 and A=0, B=1. For each combination of input, there is two possibilities transition of output: High (1) to Low (0)

and Low (0) to high (1) as shown in Table 1.

ii. The amplitude of SEU is varied until the outputs are flipped from 0 to 1 or 1 to 0 with the rising and falling times of the current pulse is fixed. The simulation is done using circuit analyser (spectre). The critical charge which corresponds to the amplitude of the current pulse that causes the state to change is obtained at different nodes and technology.

iii. Standard deviation of critical charges is calculated to observe the dispersion value of critical charge when one of the factors mentioned above changes. The responses of the state holders by observing only the change of the state holder from 1-0 change or 0-1 change can be divided into three states as shown in Figure 6 and 7:

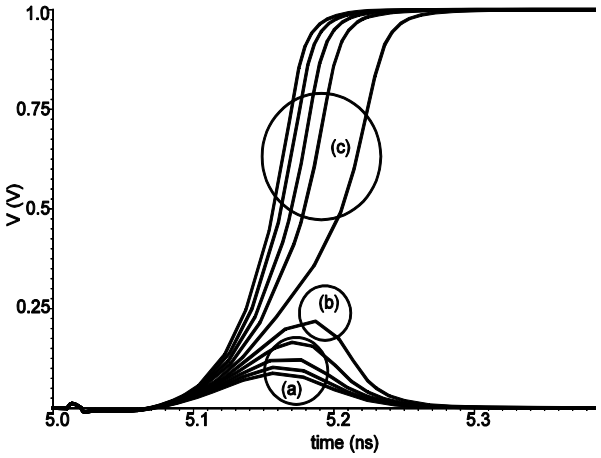

Figure 6: State holder change from low to high (0-1)

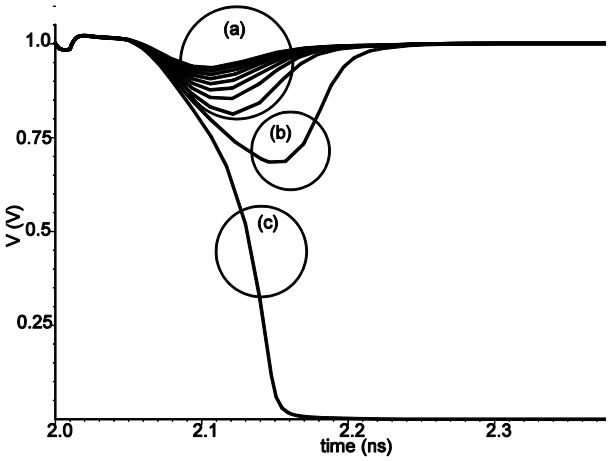

Figure 7: State holder change from high to low (1-0)

(a) No change to the state holder – There is insignificant output pulse that has been generated and does not cause any state change. It is assumed that if the generated pulse is less than 20% [9] of the input pulse such pulse can be further attenuated in the following gates and caused no further damage. This is shown in Figure 6(a) and Figure 7(a).

(b) Pulse output is generated- Over a small range of input pulse amplitude, the pulse output is generated. It is assumed that if the generated pulse is 20% [9] or more of the input pulse, such pulse can be very likely to cause the problem. This is shown in Figure 6(b) and Figure 7(b)

(c) State change – At certain amplitude of current pulse, the state holder can change its state. This is shown in Figure 6(c) and Figure 7(c)

Table 1
Combination of Inputs

Inputs	Outputs
A=1, B=0	0-1
	1-0
A=0, B=1	0-1
	1-0

III. Result and Discussion

Generally, as the technology is scaled down the transistors are very vulnerable to soft error. Figure 8-10 shows the critical charge of the injected soft error with different technology and temperature at different nodes. As temperature increases, it degrades the threshold voltage, carrier mobility and saturation velocity [10,11]. Therefore, the carrier mobility degrades and the drain current becomes lower result in the sensitivity of the node towards SEU is increased. Hence, the critical charge needed to flip the output is decreased. To observe the change in temperature variations, the process corner is set to TT with the width of the transistors are identical.

Figure 8 shows the critical charge with respect to temperature variation when the soft error is injected at node (i) The critical charges reduces by 38% for (1-0) change and by 51% for (0-1) change as the technology change from 180 nm to 90 nm. The critical charge also decreases by 29.2% for 1-0 change and 8.2% for 0-1 change as the temperature increases from $-40^0\ C$ to $100^0 C$ for 180 nm technology. Similarly for 90 nm technology, the critical charges decrease by 21.5% for 1-0 change and 9.2% for 0-1 change on the same temperature increment. From the table of standard deviation shown in Table 2, It is concluded that 180nm technology have a greater effect on temperature variation than 90 nm technology at node (i).

Table 2
Standard deviation for the soft error at node (i)

180nm (1-0)	4.9
90nm (1-0)	2.3
180nm (0-1)	1.1
90nm (0-1)	0.6

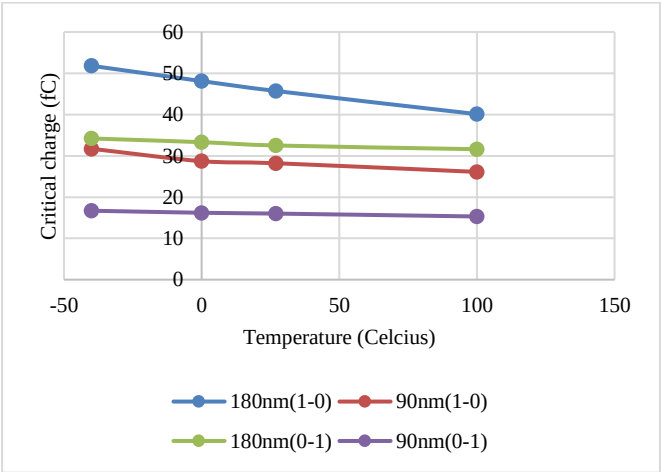

Figure 8: Temperature Variation for SIL configuration at node (i) with different technology

Figure 9 shows the critical charge with respect to temperature variation when the soft error is injected at node (ii) The critical charges reduces by 39% for (1-0) change and by 49% for (0-1) change as the technology change from 180 nm to 90 nm. The critical charge also decreases by 27.3% for 1-0 change and 10.1% for 0-1 change as the temperature increases from $-40^0\ C$ to $100^0 C$ for 180 nm technology. Similarly for 90 nm technology, the critical charges decrease by 24.5% for 1-0 change and 12.9% for 0-1 change on the same temperature increment. From the table of standard deviation shown in Table 3, It is concluded that 180nm technology have a greater effect on temperature variation than 90 nm technology at node (ii).

Table 3
Standard deviation for the soft error at node (ii)

180nm (1-0)	4.6
90nm (1-0)	2.5
180nm (0-1)	1.5
90nm (0-1)	0.9

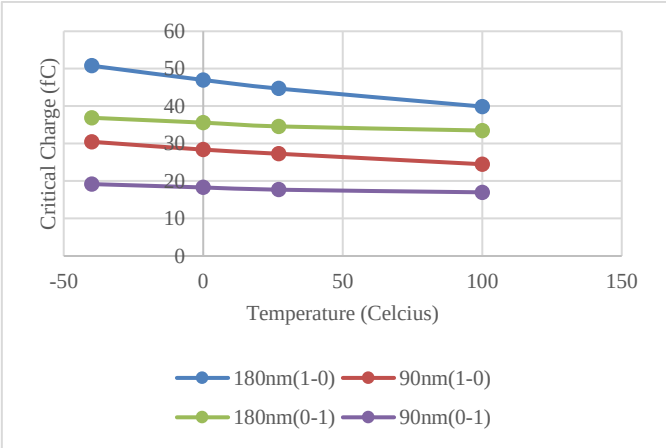

Figure 9: Temperature Variation for SIL configuration at node (ii) with different technology

Figure 10 shows the soft error is injected at node (iii) The critical charges reduces by 39% for (1-0) change and by 51% for (0-1) change as the technology change from 180 nm to 90 nm. The critical charge also decreases by 27.4% for 1-0 change and 8.2% for 0-1 change as the temperature increases from $-40^0\ C$ to $100^0 C$ for 180 nm technology. Similarly for 90 nm technology, the critical charges decrease by 23.7% for 1-0 change and 10.3% for 0-1 change on the same temperature increment. From the table of standard deviation shown in Table 4, It is concluded that 180nm technology have a greater effect on temperature variation than 90 nm technology at node (iii)

Table 4
Standard deviation for the soft error at node (iii)

180nm (1-0)	4.6
90nm (1-0)	2.5
180nm (0-1)	1.1
90nm (0-1)	0.7

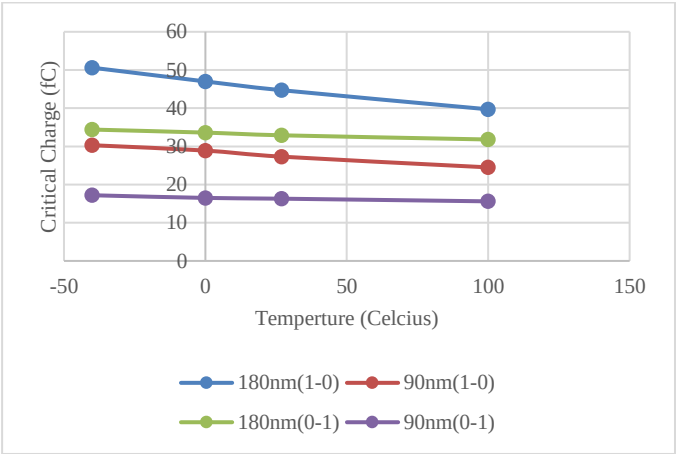

Figure 10: Temperature Variation for SIL configuration at node (iii) with different technology

IV. Conclusion

Data in digital circuit can be corrupted by the event known as single event upset (SEU) due to soft error affects digital circuit by corrupting the data in the circuit. In this paper, current pulse causing SEU is injected to every node of the different technology of C-elements. The 180 nm SIL layout has the area four times compared with the layout in 90 nm technology. By scaling down the circuit from 180 nm to 90 nm, the vulnerability due to soft error is reduced by approximately 50%. As temperature increases, it degrades the threshold voltage, carrier mobility and saturation velocity [6,7]. As a result, the drain current becomes lower and the sensitivity of the node towards SEU is increased. Hence, the critical charge needed to flip the output is decreased. The critical charge also decreases by approximately 25% for 1-0 change and 10% for 0-1 change as the temperature increases from $-40^0\ C$ to $100^0 C$. It is observed that 1-0 changes have the higher percentage changes compared with 0-1 changes. The standard deviation is higher for 180 nm compared with 90 nm technology.

Acknowledgements

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