

Hafnium Dioxide (HfO₂) as Micro-crucible Liner on GeOI for Rapid Melt Growth (RMG) Structure

N. Zainal¹, S. J. N. Mitchell² and D. W. McNeill²

¹Faculty of Electrical & Electronic Engineering, Universiti Tun Hussein Onn Malaysia (UTHM),
86400 Parit Raja, Batu Pahat, Johor, Malaysia

²School of Electronics, Electrical Engineering and Computer Science, Queens University Belfast, BT9 5AH,
Northern Ireland, United Kingdom
nurfarina@uthm.edu.my

Abstract—This paper presented an evaluation of hafnium dioxide (HfO₂) used as insulator and micro-crucible in the modification of rapid melt growth (RMG) structure. A 20 nm HfO₂ have been deposited on silicon (Si) and silicon on insulator (SOI) substrates using Atomic Layer Deposition (ALD). Samples encapsulated with HfO₂ in the RMG structure shows free from cracks and delamination even heated at higher annealing temperature (1049 °C) that observed by Scanning Electron microscopy (SEM), Transmission Electron Microscopy (TEM) and Focus Ion Beam (FIB). The quality of germanium (Ge) thin-film is characterised using micro-Raman Spectroscopy. Results show that samples with HfO₂ micro-crucible liner on Si substrate gives the Ge-Ge peak position lies at ~299 cm⁻¹, indicating that the 20 nm HfO₂ layer gives slightly tensile strain with a small shift in peak position compared to the bulk reference value of 300.2 cm⁻¹. The Raman peak position for samples on SOI substrate increased approximately 0.3 cm⁻¹ to 299.3 cm⁻¹ indicating lower stress. The Raman peak of this sample had an increased Full width at half maximum (FWHM) of ~3.9 cm⁻¹ which is believed to be mainly due to the presence of HfO₂ and scattering of Raman laser.

Index Terms—Germanium-on-Insulator (GeOI); Ge Solar Cells; Hafnium Dioxide (HfO₂); Rapid Melt Growth (RMG) Technique; Silicon-on-Insulator (SOI); Thin-film Germanium (Ge).

I. INTRODUCTION

Fabricating thin film germanium (Ge) is potentially a cost-effective way to produce energy conversion devices, yet it is not straightforward and the challenges in performing the task need to be addressed. Researchers have sought a number of possible ways to produce high-quality thin film Ge for device enhancement. Published papers claim that direct epitaxial growth of Ge on silicon (Si) can provide good crystalline Ge films for example by using a graded buffer layer [1], [2]. However, this technique suffers from dislocation defects due to the lattice constant mismatch of 4 % between Si and Ge, which result in device degradation. Having a germanium on insulator (GeOI) structure could minimise the dislocation defects between Si and Ge. However, Ge is an expensive and scarce material. In 2010 the average price for large ingot Ge per kilogram was approximately 1,200 US dollar [3]. The use of a light concentrator significantly reduces the overall expenditure for multi-junction solar cells but the major contributor (over 50 %) to the high cell cost [4] is the substrate material, which is bulk Ge. The high cost of bulk material can be avoided by exploiting technology such as GeOI. In this case, instead of using the bulk material, a

thinner Ge film can be produced thus reducing cost. It has been reported [5], [6], [7] that high-quality thin film Ge, similar to that of bulk material, could be attained by the rapid melt growth technique. Thus, by applying this approach to the current multi-junction photovoltaic cells, a cost-effective, device with high performance is anticipated to be achieved.

II. METHODOLOGY

The rapid melt growth (RMG) process uses a micro-crucible holding the molten Ge. In the fabrication process for Physical Vapour Deposition (PVD) Ge, the crucible is formed on the surface of an oxidised Si wafer with the Ge contacting the Si in seed window. The Ge is patterned into stripes and covered with a capping layer to form the micro-crucible as shown in figure 1. Rapid thermal annealing (RTA) is applied to heat the Ge above its melting point (938 °C) for a few seconds. After annealing, the Ge cools and crystallizes starting from the Si seed and continuing laterally along the crucible. The crucible can become strained due to the Ge balling phenomenon and so the capping layer was reinforced using a polycrystalline silicon (Poly-Si) layer and HfO₂. This is essential to minimise Ge balling and delamination.

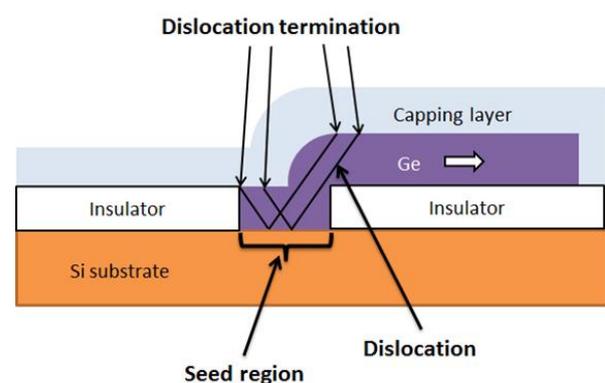


Figure 1: Dislocation termination of lattice mismatch at seed.

III. EXPERIMENTAL DETAILS

The increased attention towards high dielectric constant material (high-k) that can be employed in the gate stack of advanced MOS devices [8], [9], [10] has made HfO₂ as one of the candidates to be investigated as an insulator or micro-crucible liner in the RMG process. Most study in RMG technique to date; tend to focus on silicon dioxide (SiO₂) and silicon nitride (Si₃N₄) as insulator materials [5], [6], [7]. Only

one study has so far reported the use of HfO_2 for the RMG process, namely the comparison of insulator materials by Hashimoto et al. [11].

Test structures incorporating HfO_2 as a crucible-liner were fabricated in a similar manner to previous RMG structures as explained in the methodology section. Atomic layer deposition (ALD) was used to deposit a 20 nm HfO_2 layer at 50 nm SiO_2 . Buffered hydrofluoric acid (HF) was used to etch the SiO_2 and HfO_2 , respectively to form the seed region. A 170 nm thick Ge was sputter deposited and patterned into narrow stripes that started from the seed window and continue laterally along the HfO_2 surface. Reactive ion etching (RIE) was used to pattern the narrow Ge stripes, which were then encapsulated with 20 nm of HfO_2 . The samples were then coated with 0.5 μm thick Plasma Enhanced Chemical Vapour Deposition (PECVD) oxide and 1 μm of Poly-Si as depicted in figure 2. The quality of Ge crystalline structure is examined by micro-Raman spectroscopy with Scanning electron microscope (SEM), Focus ion beam (FIB) and Transmission electron microscopy (TEM) used for imaging.

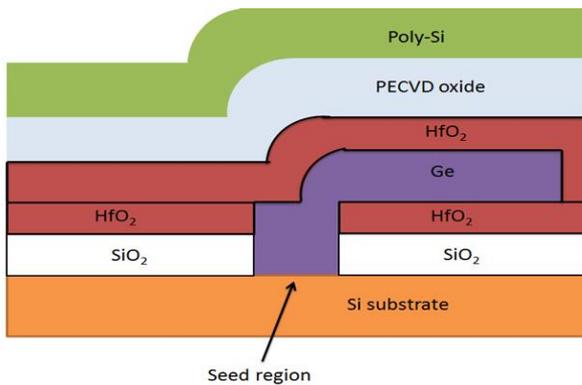


Figure 2: Schematic diagram of micro-crucible liner for RMG process (not to scale)

For crystalline quality comparison, silicon on insulator (SOI) has also been adopted as a substrate in this investigation. The aim is to observe the possibility of fabricating alternative device structure from Ge produces by the RMG process on SOI, for example for photonic applications. An advantage of SOI is that it can reduce substrate leakage to the Si bulk and minimise parasitic capacitance, which can reduce power consumption and enhance operating speed [12]. The test structures on SOI are similar to those on Si substrate as shown in figure 3, both structures were produced in parallel and heated treated using RTA.

IV. RESULTS AND DISCUSSIONS

A. Micro-crucible liner and substrate

A range of heat treatments was applied to the test sample, from 941 °C to above ≥ 1000 °C. The aim was to produce high-quality thin film crystalline GeOI using the RMG technique where samples anneal above the Ge melting point (938 °C). It was found that HfO_2 cap was difficult to etch after high annealing temperature; thus the layer remains on the sample. It is believed that the HfO_2 has been crystallised during the annealing process.

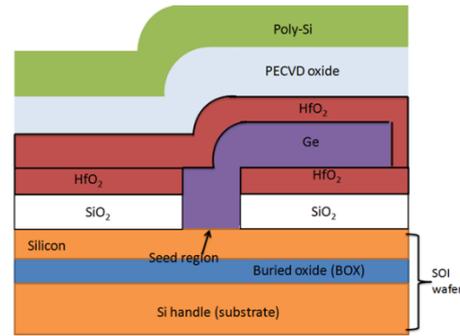


Figure 3: Schematic diagram of 170 nm Ge with SOI (not to scale)

Balasubramanian et al., [13] have also reported a similar condition where HfO_2 was unable to be etched after treated with RTA at 1000 °C for 1 second. In their case, HfO_2 was grown by Metal-Organic Chemical Vapour Deposition (MOCVD) and etched using dilute hydrofluoric acid (HF) (1:100 and 1:50) solution and they suggest that it has been crystallised during the heat treatment. They have reported that doping the HfO_2 with arsenic (As) or boron (B) could enable the etching process. However, even so, there was a 15 Å HfO_2 layer that was unable to be etched completely [13].

Figure 4 depicts an SEM micrograph of a test sample showing a rougher surface. The micrograph also shows that no cracks were observed at the edge of the seed window for 60 μm to 400 μm long Ge stripes with 3 to 4 μm wide. These results were observed in all samples either on Si or SOI substrates. The samples with HfO_2 as crucible liner have also been analysed with FIB and TEM. In this case, FIB was used to cut and milling on a specific region of the samples hence, inspected using TEM.

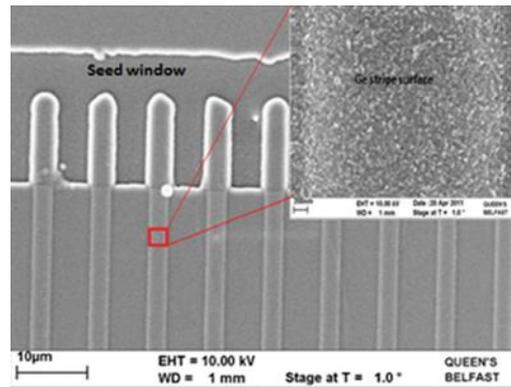


Figure 4: Micrograph of Ge on HfO_2 with rougher surface after RTA at 1049 °C with capping removal.

Figures 5 and 6 show the wavy surfaces of the Ge stripes from the RMG process at 1049 °C. These cross-sections show similarity to Ge on SiO_2 sample examined earlier [7]. It is believed the Ge wavy surface formed due to the Ge balling phenomenon, where it shrinks during melting and expand when solidifying, resulting in more strain on the capping layer thus, cracks and delamination can occur. However, by having HfO_2 as a micro-crucible liner on the RMG structure have to make the capping layer rigid enough to hold the Ge during balling phenomenon without any sample destruction. It is also shown that combination of Poly-Si cap and HfO_2 crucible on Ge is more robust than PECVD oxide crucible on Ge layer [7] where it can withstand above 1000 °C annealing temperature. Thus, better crystalline quality thin film Ge is anticipated to be obtained.

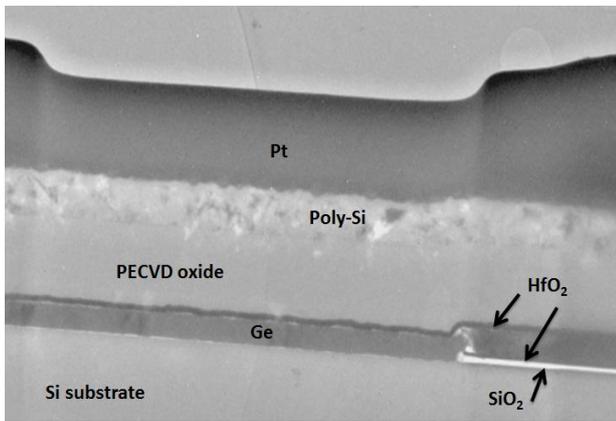


Figure 5: Cross-section of seed window with capping layers cut by FIB and observed using TEM

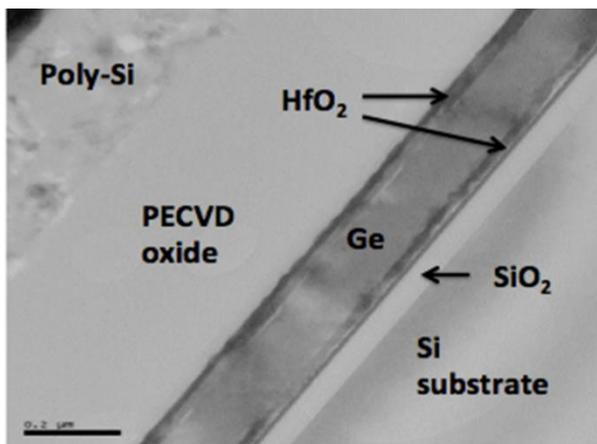


Figure 6: Cross-section of Ge stripe annealed at 1049 °C cut by FIB and observed using TEM

B. Crystalline quality of RMG germanium on different substrate examine by micro-Raman Spectroscopy

The crystal quality of the Ge stripes was assessed by micro-Raman spectroscopy for a sample of Si and SOI substrates. The Raman measurement was performed through the 20 nm HfO_2 capping layer. In order to examine whether the HfO_2 on Ge affects the Raman peak position and full width at half maximum (FWHM) or linewidth, two control samples were prepared. First, a control sample with 20 nm thick HfO_2 deposited on bulk Ge with no RTA and secondly, a 20 nm thick HfO_2 deposited on bulk Ge heated to 940 °C. Results show that the Ge-Ge peak position lies at 299.7 cm^{-1} for both cases; indicating that the 20 nm HfO_2 layer gives slightly tensile strain with a small shift in peak position compared to the bulk reference value of 300.2 cm^{-1} . As expected, the rougher surface of HfO_2 results in an increased Raman linewidth with average FWHM of 3.75 cm^{-1} .

Test samples on Si and SOI substrates were measured along the stripes with 2 μm of step size in vertical line mapping using a red laser. The average values of Raman peak position and FWHM versus annealing temperatures are plotted in Figure 7 and 8 for samples with Si and SOI substrates. The results have similar trends to Ge on SiO_2 , where better crystalline quality with reduced FWHM is produced at high annealing temperature [7]. The presence of HfO_2 and its rougher surface is believed to have caused scattering of Raman laser, which results in minor variations of Raman peak position and FWHM.

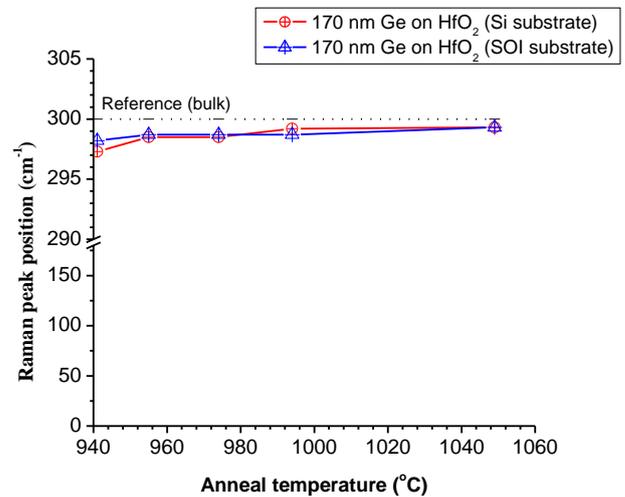


Figure 7: Average values of Raman peak position versus anneal temperatures for samples on Si and SOI substrates

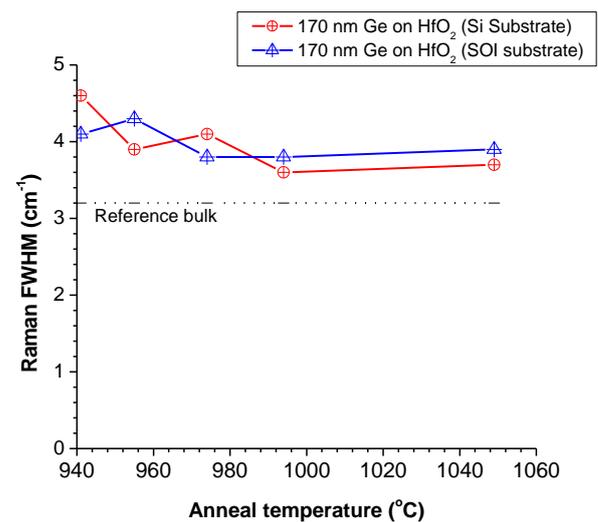


Figure 8: Average values of Raman FWHM versus anneal temperatures for samples on Si and SOI substrates

As expected, all Ge on HfO_2 samples has a lower longitudinal optical (LO) Ge-Ge Raman peak position ($\sim 299 \text{ cm}^{-1}$) than bulk Ge (300.2 cm^{-1}). This indicates that the Ge is under tensile stress which is believed to be due to differences in the thermal expansion coefficients of materials in the micro-crucible structure. The rougher HfO_2 surface observed on test samples has caused the Raman peak to be slightly wider in comparison to Ge on SiO_2 as reported elsewhere [7]. A similar effect was reported earlier in this section for the control samples.

For the test structure on SOI substrate, a higher annealing temperature was performed with the sample heated to 1049 °C. At this higher temperature, the samples remained free from cracks and delamination. The Raman peak position increased approximately 0.3 cm^{-1} to 299.3 cm^{-1} indicating lower stress. The Raman peak of this sample had an increased FWHM of $\sim 3.9 \text{ cm}^{-1}$ which are believed to be mainly due to the presence of HfO_2 and scattering of Raman laser. This demonstrates that the crystalline Ge stripes produced from RMG technique have a slight tensile strain in the test structure, due to the different expansion coefficient (TEC) between Ge and crucible materials. This tensile strain may have a significant impact on the characteristics of Ge semiconductor devices. The tensile strain will influence of

band structure which will result in an increase of the electron mobility and therefore enhance the optoelectronics properties [12]. Thus, this tensile strain could be beneficial for the production of solar energy conversion devices.

V. CONCLUSION

HfO₂ has been evaluated as an insulator and crucible material. It has shown that providing this material as a crucible liner has removed the micro-cracks at the edge of seed window. Hence, Ge stripes are free from major defects such as cracks and delamination even at higher crystal growth temperature. The results of this investigation have also shown an improvement in the thermal annealing process as compared to the Ge on SiO₂ [7]. Prior to this work, the combination of Poly-Si cap and HfO₂ crucible liner had not been reported. This interesting finding has thus added to the growing body of literature on the RMG process for obtaining high-quality crystalline Ge. Moreover, the modification of the basic RMG structure has demonstrated that high-quality thick Ge stripes can be fabricated; with good quality crystalline, Ge yielded at high annealing temperature. Hence this RMG technique has the possibility to be applied for the development of future Ge photovoltaic devices. In order to measure electrical characterisation of crystalline Ge produced by the RMG process, metal contacts are required to be formed on Ge. Results demonstrate that the HfO₂ cap was difficult to etch after higher heat treatment. Therefore, it was decided not to deposit HfO₂ on top of germanium in forthcoming fabrication to enable metal contacts to be formed.

ACKNOWLEDGMENT

This work is under the financial support short-term grant (Vot U352) of Universiti Tun Hussein Onn Malaysia and in collaboration with Queen's University Belfast (QUB), Northern Ireland, United Kingdom. The authors wish to thank Dr T Perova, Trinity College Dublin for valuable input on the Raman analysis.

REFERENCES

- [1] S. Luryi, A. Kastalsky, and J. C. Bean, "New infrared detector on a silicon chip," *IEEE Trans. Electron Devices*, vol. 31, no. 9, pp. 1135–1139, Sep. 1984.
- [2] K. Tani, S. Saito, Y. Lee, K. Oda, T. Mine, T. Sugawara, and T. Ido, "Light Detection and Emission in Germanium-on-Insulator Diodes," *Jpn. J. Appl. Phys.*, vol. 51, p. 04DG09, Apr. 2012.
- [3] K. Salazar and M. K. McNutt, "Metal Prices in United States through 2010," [Online] Available: <http://pubs.usgs.gov/sir/2012/5188/sir2012-5188.pdf>.
- [4] M. Bosi and G. Attolini, "Germanium: Epitaxy and its applications," *Prog. Cryst. Growth Charact. Mater.* vol. 56, no. 3–4, pp. 146–174, Sep. 2010.
- [5] Y. Liu, M. D. Deal, and J. D. Plummer, "High-quality single-crystal Ge on insulator by liquid-phase epitaxy on Si substrates," *Appl. Phys. Lett.*, vol. 84, no. 14, p. 2563, 2004.
- [6] M. Miyao, K. Toko, T. Tanaka, and T. Sadoh, "High-quality single-crystal Ge stripes on quartz substrate by rapid-melting-growth," *Appl. Phys. Lett.*, vol. 95, no. 2, p. 022115, 2009.
- [7] N. Zainal, S.J. N Mitchell, D. W. McNeill, M. F. Bain, B. M. Armstrong, P. Baine, D. Adley, and T. S. Perova, "Characterization of Rapid Melt Growth (RMG) Process for High Quality Thin Film Germanium on Insulator," *ECS Trans.*, vol. 45, no. 4, pp. 169–180, 2012.
- [8] J. C. Kim, J. S. Heo, Y. S. Cho, and S. H. Moon, "Atomic layer deposition of an HfO₂ thin film using Hf(O-iPr)₄," *Thin Solid Films*, vol. 517, no. 19, pp. 5695–5699, Aug. 2009.
- [9] H. R. Huff, A. Hou, C. Lim, Y. Kim, J. Barnett, G. Bersuker, G. A. Brown, C. D. Young, P. M. Zeitzoff, J. Gutt, P. Lysaght, M. I. Gardner, and R. W. Murto, "High-k gate stacks for planar, scaled CMOS integrated circuits," *Microelectronic Engineering*, vol. 69, pp. 152–167, 2003.
- [10] S. Murad, P. Baine, and J. Montgomery, "Electrical and Optical Characterization of GeON Layers with high-k Gate Stacks on Germanium for Future MOSFETs," *ECS Trans.*, vol. 45, no. 3, pp. 137–144, 2012.
- [11] T. Hashimoto, C. Yoshimoto, T. Hosoi, T. Shimura, and H. Watanabe, "Fabrication of Local Ge-on-Insulator Structures by Lateral Liquid-Phase Epitaxy: Effect of Controlling Interface Energy between Ge and Insulators on Lateral Epitaxial Growth," *Applied Physics Express*, vol. 2, p. 066502, May 2009.
- [12] T.-P. Ngo, M. El Kurdi, X. Checoury, P. Boucaud, J. F. Damlencourt, O. Kermarrec, and D. Bensahel, "Two-dimensional photonic crystals with germanium on insulator obtained by a condensation method," *Applied Physics Letters*, vol. 93, no. 24, p. 241112, 2008.
- [13] M. Balasubramanian, L. K. Bera, S. Mathew, N. Balasubramanian, V. Lim, M. S. Joo, and B. J. Cho, "Wet etching characteristics and surface morphology evaluation of MOCVD grown HfO₂ film," *Thin Solid Films*, vol. 462–463, pp. 101–105, Sep. 2004.