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DESIGN AND SIMULATION OF A HIGH PERFORMANCE CMOS VOLTAGE DOUBLERS USING CHARGE REUSE TECHNIQUE

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Abstract

Voltage doubler (VD) structure plays an important role in charge pump (CP) circuits. It provides a voltages that is higher than the voltage of the power supply or a voltage of reverse polarity. In many applications such as the power IC and switched-capacitor transformers. This paper presents the design and analysis for VD using charge reuse technique CMOS 0.35µm tech. with high performance. Bootstrapped and charge reuse techniques is used to improve performance of integrated VD. Charge reusing method is based on equalizing the voltages of the pumping capacitances in each stage of CP. As a consequence, it reduces the load independent losses, improve the efficiency. Simulation using Orcad is applied for various VD structures shows improvement in charge reuse technique compared with existing counterpart. The results obtained show that the VD can be used in a wide band frequencies (0-100 MHz) or greater. The charge reuse VD circuit provided a good efficiency about (87.6%) and (83.5%) for one stage and two stage respectively at pump capacitance of 57pf, load current of 1mA, frequency of 10 MHz and supply voltage is 3.5 V compared with one stage and two stage of a latched VD are (85.4%) and (80%) respectively.

Keywords: Latched VD, Charge reuse VD, Pump capacitance, Power losses.

1. Introduction

Charge pumps are power converters that convert the supply voltage to higher or lower constant voltages. CPs transfer charge packets from the power supply to the output terminal using capacitors and switches only to generate the required voltage level [1]. The VD usually consists of two latched CMOS pairs in each stage. The buck converter reduces the dc voltage. In a similar topology known as the boost converter, the positions of the switch and inductor are interchanged.

Nomenclatures

C	Pumping capacitance, pf
Cb	Bootstrapped charge capacitance, pf
f	Input clock frequencies, Hz
I_o	Load Current
I_{DD}	Current consumption, A
N	NMOS MOSFET transistor
NB	PMOS MOSFET transistor
V_{DD}	Input voltage, Volt
V_{out}	Output voltages, Volt

Greek Symbols

α,β	Parasitic capacitance fabrication factor, deg.

Abbreviations

CP	Charge Pump
PLD	Load Dependent Losses
PLI	Load Independent Losses
VD	Voltage Doubler

This converter produces an output voltage that is greater in magnitude than the input voltage. [1].

The drop of the output switches can be eliminated by using VD circuits. It uses only two non-overlapping phases (V_1 and V_2). The VD reduced the output voltage ripple. Moreover, the voltage across each transistor is never higher than the supply voltage V_{DD}. This shows a unique design challenges in terms of power efficiency, device reliability, driving capability, and circuit performance. Figure 1 shows necessity of doubler in CP circuits [2]. The overdrive voltage decreases at high output current causing the output resistance to rise due to higher switch resistance, thus increasing resistive power losses, reducing efficiency and driving capability. The increasing efficiency of the CP circuits not only in battery-powered systems. The driving capability involves a wide range of load currents and output voltages that are desired. However, it is of particular importance that CPs are designed to function effectively for certain steady-state operating points with minimum silicon area [3].

The limitation of the conventional VD CPs is driving capability that represented a short-circuit currents and threshold voltage drop of the transistors [2]. The resulting short-circuit currents can be reduced by exploiting two parallel stages to generate control signals of the main transfer switches, or by using bootstrapping the PMOS switches. In these implementations, at high output currents, the voltage driving the switches decreases, therefore, reducing both the driving capability and efficiency. To overcome these limitation, a unconventional boosting technique is used to control switches is suitable for cascaded VD operating at low supply voltages. The solution for this is by enhancing the driving capability and allows the use of low voltage devices, but does not eliminate short-circuit losses.

Recently, Hu and Chang [4] proposed an output voltage model by the charge transfer waveforms for CP gain increase circuits. The authors assumed zero on-resistance of the transfer transistors. However, as supply voltages trend lower or loading current trends higher, the development of output voltage models that consider the more accurate on-resistance of transistors becomes important.

In [5] Chien-Pin provided a detailed accurate analytical models of the output voltage and the power efficiency of VD and PMOS CP are derived using dynamic charge transfer waveforms and charge balance methods, respectively. The proposed models are more accurate than the other existing models. The model-generated values agree well with simulations and measurements for these two CP using 0.18-µm CMOS technology. The expressions for the output voltages prove that the PMOS CP can provide more output current without a significant increase in the sizes of transistors. The 4-stage VD and the proposed PMOS CPs were designed with threshold voltages of 0.44, −0.495, and −0.73 V for NMOS, PMOS, and high-voltage PMOS transistor, respectively. Both CPs used the same transistor sizes, f = 10 MHz, I_o = 50µA, V_{DD}=1.8 V and C = 5pf for comparison with the proposed charge reuse circuits in this paper was used in 0.35-µm CMOS.

The VD circuits were designed by using charge reuse technique, it was provided high performance, increased in conversion efficiency, output voltages, and power gain, also reduced in dynamic power losses and ripple output voltage. The proposed design circuits is based on 0.35-µm process. The results obtained are very good conversion efficiency and can be used at frequency 100 MHz for charge reuse VD compared with latched and bootstrapped CP circuits.

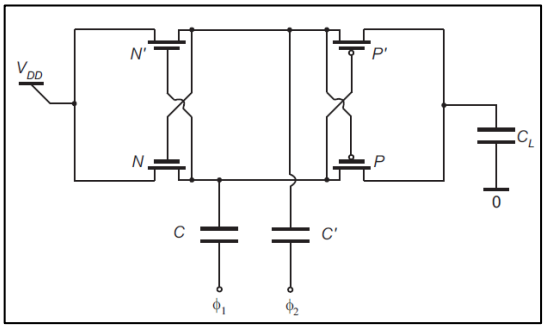

Fig. 1. Block diagram of doubler charge pump circuit.

2. Charge Pump Voltage Doubler Circuits

The analytical optimization method is determined to evaluate the voltage gain, the output resistance and the conversion efficiency parameters of integrated charge pumps. An optimization method is developed to improve the circuit performance by capacitor sizing based on area constraints. Several charge pumps structures are optimized and compared, includes the losses due to devices parasitic. The charge pump voltage doubler is suitable structure for integration. In order to improve performance and conversion efficiency, the switch bootstrapping and charge reuse techniques are used as well as conventional (latched) voltage doublers [6].

The output voltage ripple (V_r) can be reduced by splitting the CP in two parts each with half the total capacitance and feeding the load in a different half period

[7] as depicted in Eq. (1). This configuration, called double CP, is usually implemented as cascade connection of voltage doublers [6], which need two clock phases instead of four. As shown in Fig. 2 each modular stage is made of two latched CMOS pairs (N_1, P_1, N_2, and P_2), two transfer capacitors (C_1, C_2), and two drivers (N_3, P_3, N_4, and P_4), and does not need dedicated bootstrap drivers. CPs transfer charge packets from the power supply at a voltage V_{in} to an output N-stage terminal at a higher voltage V_{out}. The transfer capacitors of each stage are alternately charged to the voltage of the previous stage and then boosted by V_{DD} to charge the next stage at a higher voltage. The complementary voltage swings on the internal nodes are used to control the switches of opposite branches. Since the maximum voltage rise from V_{in} to V_{out} is V_{DD}, the voltage across each device is never higher than V_{DD} and low voltage MOS switches can be used.

In steady state, the operation of the voltage doubler of Fig. 2 is as follows, during the first half cycle ($V_1 = V_{DD}$ and $V_2 = 0$), transistors (N_2, N_4, P_1 and P_3) are ON, and transistors (N_1, N_3, P_2 and P_4) are OFF, transfer capacitor C_1 is charged to V_{in} through N_2 and N_4, while transfer capacitor C_2 is boosted to $V_{in} + V_{DD}$ through P_1 and P_3. During the second half cycle, and transistors (N_1, N_3, P_2 and P_4) are turned ON, and transistors (N_2, N_4, P_1 and P_3) are turned OFF, transfer capacitor C_2 is charged to V_{in}, while transfer capacitor C_1 is boosted to charge next stage to $V_{in} + V_{DD}$. Therefor the ripple output voltage may be given as [2]:

$$V_r = \frac{I_o}{2fC_L} \tag{1}$$

where I_o is the loading currents, C_L is the load capacitance, and f is the input clock signal frequencies.

The output voltage of an N-stage voltage doubler CP based on the assumption of zero turn-on resistance of the switching transistors can be expressed in Eq. (2) [7].

$$V_{out} = (1 + N)VDD - \frac{NI_O}{fC} \tag{2}$$

where C is the pumping capacitance, and V_{DD} is the supply voltage. However, in low voltage or high output current applications, the on-resistance of switching transistors is increased and cannot be neglected due to the low (Gate to Source voltage) V_{gs} of switching transistors. By including the on-resistance (R_{ON}) in Eq. (2), the output voltage has been reported as depicted in Eq. (3).

$$V_{out} = (1 + N)VDD - \frac{NI_O}{fC} \coth\left(\frac{1}{2fR_{ON}C}\right) \tag{3}$$

In order to prevent short-circuit currents and the reduced current driving capability observed in the conventional voltage doubler, a new modular bootstrapping technique that allows full control on MOS switches is used. The circuit in Fig. 3 provides control the timing of the switch transitions (therefore preventing short-circuit losses) and also control the gate voltage swings (therefore improving driving capability). Having same pass transistors, transfer capacitors, drivers, and non-overlapping phases as the conventional one, the proposed circuit includes an NMOS cross-coupled clock booster (NB_1, NB_2, Cb_1 and Cb_2) driven by (V_1 and V_2) and a PMOS cross-coupled clock booster (PB_1, PB_2, Cb_3 and Cb_4) driven by ($V_{1\text{-}bar}$ and $V_{2\text{-}bar}$).

The design of a voltage doubler stage with charge reuse is shown in Fig. 4. The equalization switch controlled by a NOR circuit brings both capacitances (C_1, C_2) to $V_{DD}/2$ before each switch event. Therefore the amount of charges drawn from the power supply for charging parasitic capacitances is half the amount needed by the conventional circuit. As a consequence, charge reusing approach reduces the load independent losses (P_{LI}) by a factor two. Circuit analysis confirms that the input conductance (G_I) of the VD CPs with charge reuse is half that of conventional voltage doubler CPs as expressed in Eq. (4). Assume the parasitic factor of capacitance fabrication are α = 0.015 and β = 0.01. Therefore the input conductance may be given as:

$$G_I = \frac{1}{2} * f * C * \frac{\alpha + \beta + \alpha\beta}{(1+\beta)} \tag{4}$$

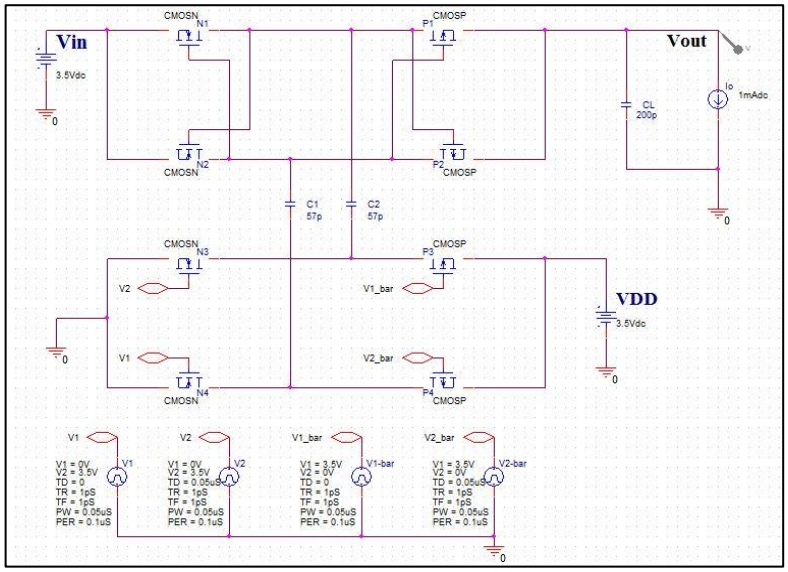

Fig. 2. One stage latched voltage doubler circuit.

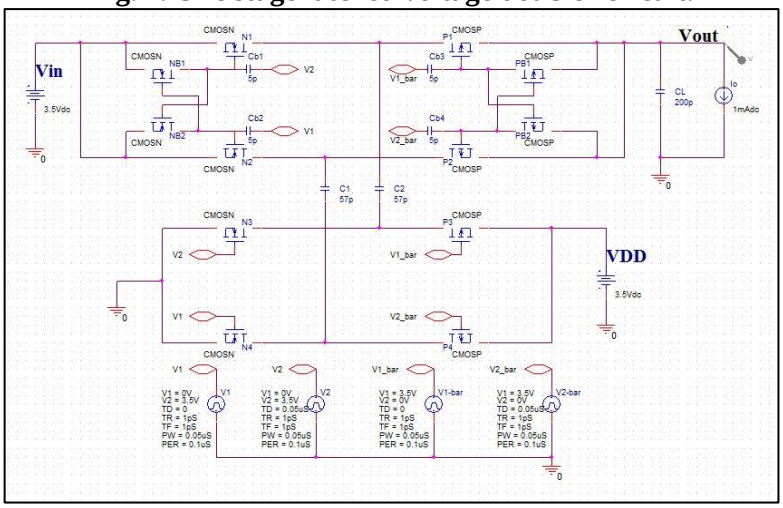

Fig. 3. One stage bootstrapped voltage doubler.

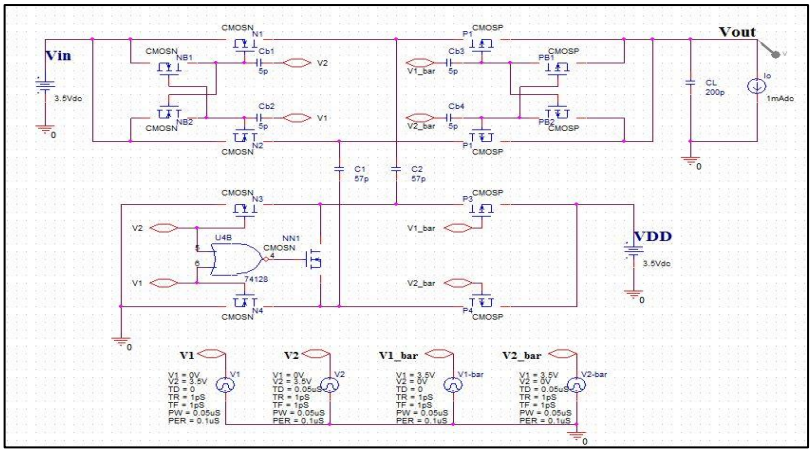

Fig. 4. One stage bootstrapped voltage doubler with charge reuse.

3. Power Losses in Charge Pumps

The operation of charge pumps is to transfer charge packets from the power supply at a voltage V_{DD} to an output terminal at a higher voltage V_{out}. During this operation, CPs dissipate a portion of the input power and may reduce the benefit of scaling down the supply voltage down. Power losses arise mainly from capacitor charging and discharging losses, resistive conduction losses, and losses due to parasitic capacitances and short-circuit currents. The main power losses are described by a simple model and can be divided into load dependent losses and load independent losses [8].

3.1. Load-dependent losses

Load-dependent losses (P_{LD}) are revealed when the charge pump is connected to a load and the output voltage decreases in the presence of a load current $I_o > 0$. These losses are modeled through a non-zero equivalent output resistance (R_O) and the corresponding power dissipation is evaluated by Eq. (5).

$$P_{LD} = R_o * {I_o}^2 \tag{5}$$

3.2. Load-independent losses

Load independent losses (P_{LI}) are revealed when the CP is not connected to any load and it still dissipates power. These losses mostly arise from charging and discharging parasitic capacitances and are also called dynamic losses. They are modelled through a non-zero equivalent input conductance (G_I) and the corresponding power dissipation is evaluated by Eq. (6):

$$P_{LI} = G_I * {V_{DD}}^2 \tag{6}$$

The energy efficiency is defined as the average power delivered to the load divided by the average of input power is given by Eq. (7).

$$\eta = \frac{P_o}{P_{in}} = \frac{V_{out} * I_o}{P_o + P_{LD} + P_{LI}} \tag{7}$$

where P_o is the power delivered to the load and P_{in} is the average of input power.

4. Simulation Results

The voltage doubler charge pump circuits are designed and simulated using OrCad software such as one and two stage of the latched VP, bootstrapped and charge reuse voltage doubler CP. The MOS switches and poly-diffusion capacitors used in a standard 0.35-μm CMOS technology. The analysis was simulated in this work allows the calculation of the voltage gain (A), output resistance (R_O), and input conductance (G_I) and consequently the major power losses of any CP circuits represented resistive and dynamic power losses P_{LD} and P_{LI} respectively can be evaluated. Moreover, charge reuse technique application in CP circuit design will provide a significant reduction in dynamic power losses as well as improvement the overall efficiency. Also it is applied to double CP circuit structures in addition to bootstrapped structure. To verify the improvements achieved by the proposed switch bootstrapping technique and the charge reusing technique, voltage doublers with the proposed techniques. All voltage doublers CP circuits were designed under same specifications which include 57pF stage capacitance, 3.5V supply voltage, same clock frequency, and the same sizes of charge transfer switches.

Performance of the one-stage bootstrapped VD Fig. 3 and the one-stage latched VD shown in Fig. 2 is compared. Both VD are designed to achieve a voltage gain of A=2 and to deliver an output current from 0 A to 8 mA. Fig. 5 presents the simulated output characteristic at f = 10 MHz. Simulation results show that the bootstrapped VD provides an open-circuit output voltage of 3.35V, as compared 2.4 V provided by the latched VD at I_o = 5 mA because short-circuit losses are prevented and parasitic capacitances of the pass transistors do not increase the value of β at the voltage doubler internal nodes in the bootstrapped.

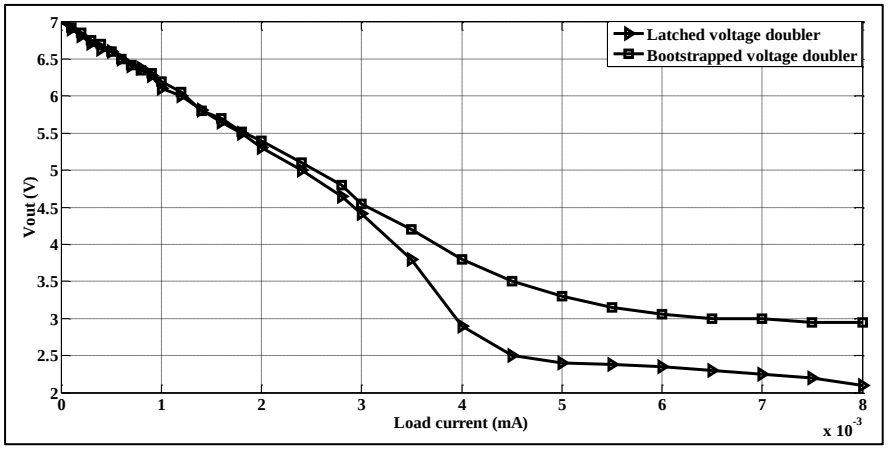

Fig. 5. Output characteristics of a one stage latched and bootstrapped voltage doublers as a function of load current I_o when N=1, V_{DD}=3.5 V.

The simulated output resistance is nearly constant (R_O=878Ω), while the output resistance of latched VD increases significantly.

The efficiency as a function of the load current is shown in Fig. 6 for both VD at f = 10 MHz. The maximum efficiency of the bootstrapped VD is 86.4%

when I_o = 1 mA, while the maximum efficiency of the latched VD is 85.4% when I_o=1 mA. It can be also seen from this figure that any frequency, the efficiency of the bootstrapped doubler is improved at both low and high load currents. At high load current, also the efficiency is significantly improved as well because of the nearly constant output resistance. Two-stage bootstrapped CP and two-stage latched VD are designed and simulated to have a voltage gain of A = 3 and deliver an output current from 0 A to 8 mA. Figure 7 presents a comparison for the variation of the output voltage as function of the load current (I_o) between the two VD. The maximum output is 2.85 V for the two stage bootstrapped VD and 1.42 V for the two stage latched VD at I_o = 5 mA. It is also seen that the bootstrapped VD is able to guarantee a constant value of (R_O = 1.75 KΩ) at (f = 10 MHz) for the whole output current range. The efficiency as a function of the load current is shown in Fig. 8 for both voltage doublers at f = 10 MHz. The maximum efficiency of the bootstrapped CP is about 82% at I_o = 1 mA, while the maximum efficiency of the latched CP is 80.7% when I_o = 1 mA at f = 10 MHz.

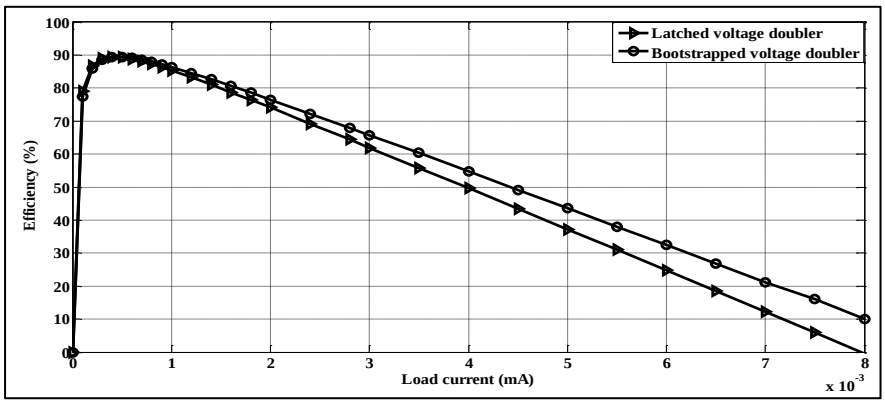

Fig. 6. Conversion efficiencies of a one stage latched and bootstrapped voltage doublers as a function of load current I_o when N=1, V_{DD}=3.5 V.

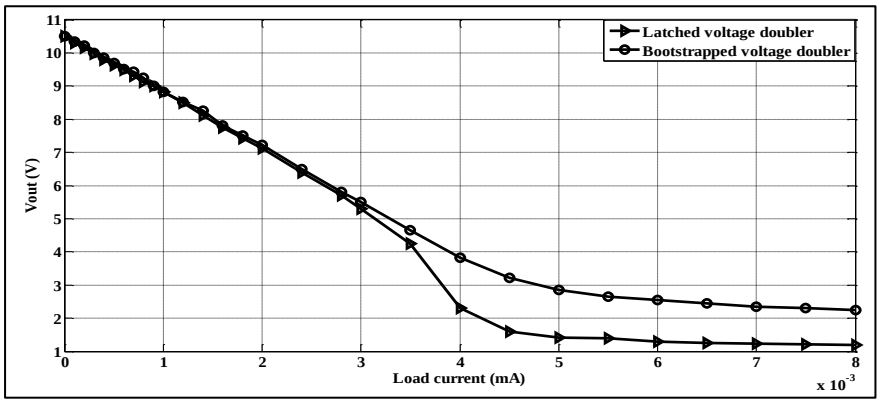

Fig. 7. Output characteristics of a two stage latched and bootstrapped voltage doublers as a function of load current I_o when N=2, V_{DD}=3.5 V.

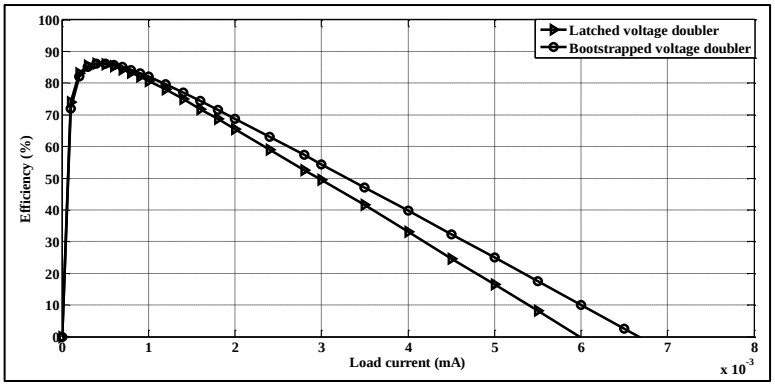

Fig. 8. The efficiencies of a two stage latched and bootstrapped VD as a function of load current I_o when N=2, V_{DD}=3.5 V, f=10 MHz and C=57 pf.

To evaluate the impact of charge reuse technique, a two stage bootstrapped voltage doubler with charge reuse are designed and compared to the two stage voltage doubler. The output characteristic and efficiency comparison for different load conditions are shown in Figs. 9 and 10 at 10 MHz. The simulated output characteristics for both voltage doublers are identical, because the (f, C) product and the number of stages are fixed. The simulated conversion efficiency of the two-stage bootstrapped voltage doubler and of the two-stage bootstrapped voltage doubler with charge reuse as a function of the load current is shown in Fig. 10. The efficiency of the bootstrapped voltage doubler with charge reuse is improved at low and moderate load currents compared with other models. The charge reuse technique resulted for these VD charge pump circuits gives a significant improvement for the desired values compared with conventional methods has been used in [3, 6] are shown in Table 1. It can be seen from the table that charge reuse technique results is best.

Table 1. Results comparison between present work and other papers.

	Model [2]	**Model [6]**	**Present Work**
Fabrication technology	0.18-µm CMOS process	0.135-µm CMOS process	0.35-µm CMOS process
Freq. range, *f* (MHz)	(1-10)	(1-10)	(1-100)
Number of stages, *N*	2	4	2
Input Voltage, V_{DD} (V)	1.8	1.35	3.5
Technical used	Bootstrapped and charge reuse	Bootstrapped technique	Charge reuse technique
Out. current, I_o (mA)	(0-2)	300 µA	(0-8)
Design current (mA)	0.5	0.3	1
Pump capacitance (pf)	262.5	32	57
Conv. efficiency (%)	79.83	68	87.6

Charge reusing improves the overall conversion efficiency substantially because a significant amount of the charges normally wasted through parasitic capacitances is reused. The maximum efficiencies of the charge reuse voltage doubler are 87.55% and 83.5% for one stage and two stages respectively. However, the overall reduction in load-independent losses is less than 50% of theoretical reduction, because there are diminishing effects caused by additional power losses from the charge reuse circuit.

A significant advantage of the proposed voltage doubler is the faster rise time of the output voltage at the start-up, the simulated start-up for the two-stage bootstrapped voltage doubler is 1.26 μs compared with 2.26 μs for the two-stage latched voltage doubler, i.e. the rise time of the bootstrapped doubler is reduced by 47% compared to the conventional one. The improvement in start-up time results resulted from the smaller on resistance of the bootstrapped switches, because the switches have gate voltage swings varying from 0 to V_{DD}.

Voltage analysis of a one stage bootstrapped voltage doubler and two stage bootstrapped voltage doublers. On varying the supply voltage change is observed in output voltage. Output voltage increases with increase in supply voltage, supply voltage is varied from 1 V to 10 V. Figure 11 shows the simulated output voltages for the one and two stage bootstrapped voltage doubler with various supply voltages when load current is 1 mA, pumping capacitance is 57pf and the input clock frequency 10 MHz. Figure 12. and 13 present the simulated power conversion efficiencies of a one stage latched voltage doubler and bootstrapped voltage doubler with charge reuse as a function of supply voltage (V_{DD}) when load current (I_o = 1 mA), f = 10 MHz, C = 57 pf, N = 1 and N = 2 respectively.

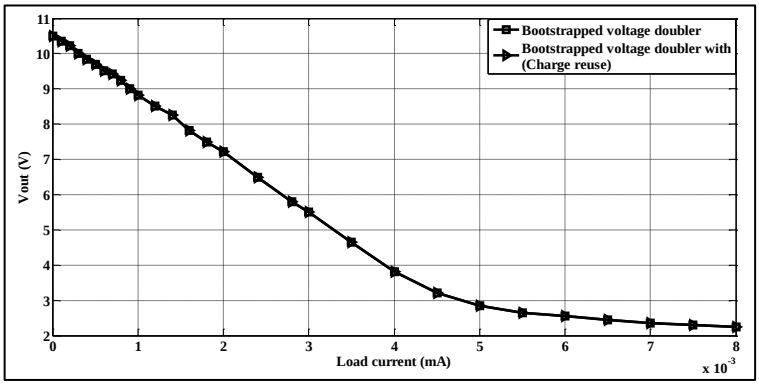

Fig. 9. Output characteristics of a two stage bootstrapped VD and charge reuse bootstrapped voltage doubler circuit as a function of load current.

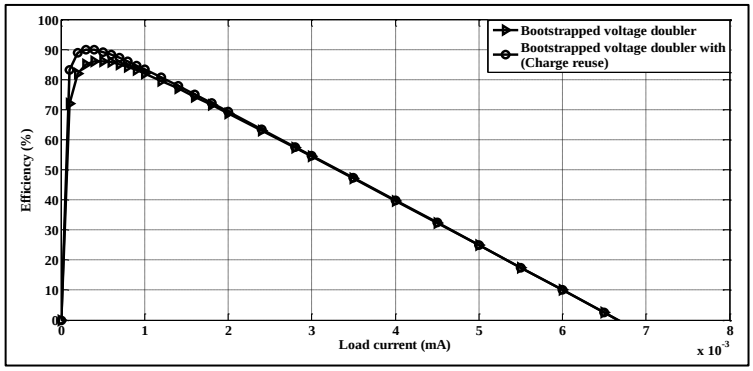

Fig. 10. Conversion efficiencies of a two stage bootstrapped VD and charge reuse bootstrapped voltage doubler circuit as a function of load current (I_o).

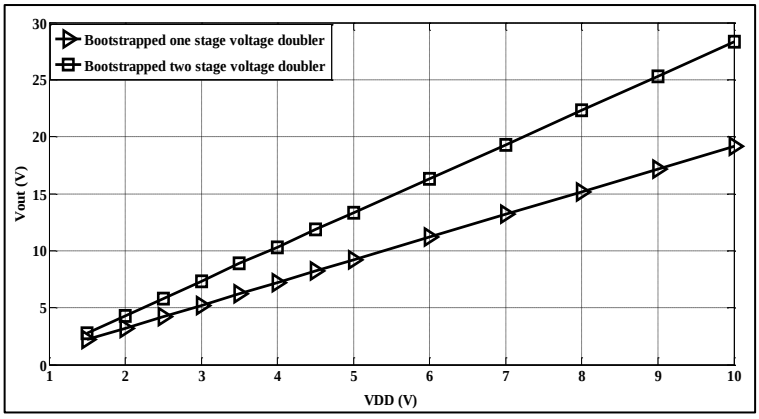

Fig. 11. Output voltages of a one stage and two stage bootstrapped voltage doublers as a function of supply voltage when I_o=1 mA, f=10 MHz.

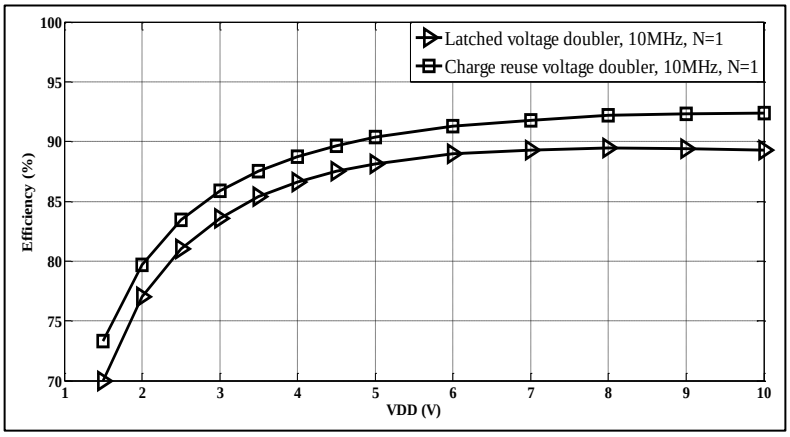

Fig. 12. Conversion efficiencies of a one stage latched VD and bootstrapped VD with charge reuse as a function of V_{DD} when I_o=1 mA.

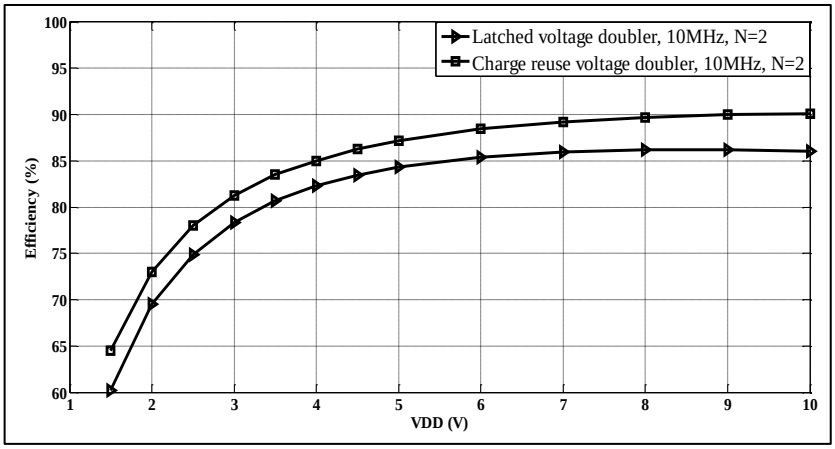

Fig. 13. Conversion efficiencies of a one stage latched VD and bootstrapped VD with charge reuse as a function of V_{DD} when I_o=1 mA

The VD circuits can be used in a wide band range of frequencies about 100 MHz or greater. Figure 14 presents the simulated output voltages of the two stages latched VD and bootstrapped VD with charge reuse versus input clock frequency with 3.5V supply voltage, 57pf pump capacitance and 1 mA load current. It can be seen from this figure that the charge reuse VD has an output voltages higher than latched VD at different frequency. Figure 15 shows the simulated conversion efficiencies of a one stage latched VD, bootstrapped VD and charge reuse VD with respect to change in frequencies. The two stage bootstrapped VD with charge reuse has a power efficiencies is less than the one stage bootstrapped VD with charge reuse about 10% as shown in Fig. 16.

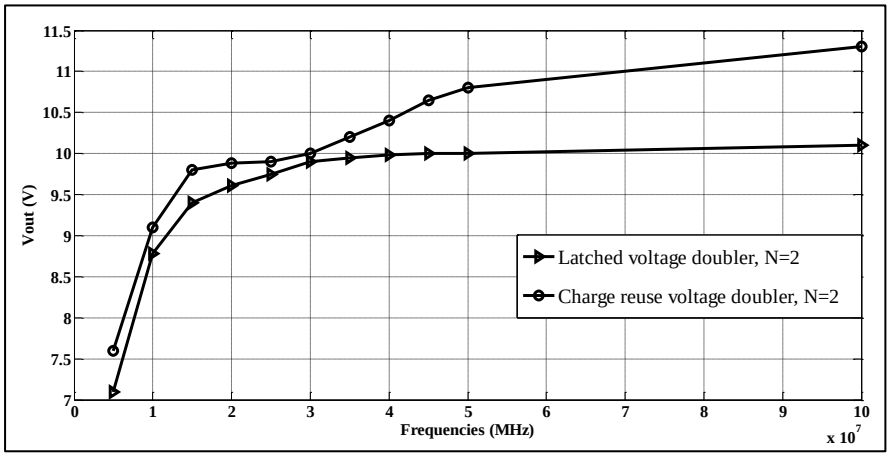

Fig. 14. Output voltages of a two stage latched and charge reuse VD as a function of frequencies when I_o=1 mA, V_{DD}=3.5 V.

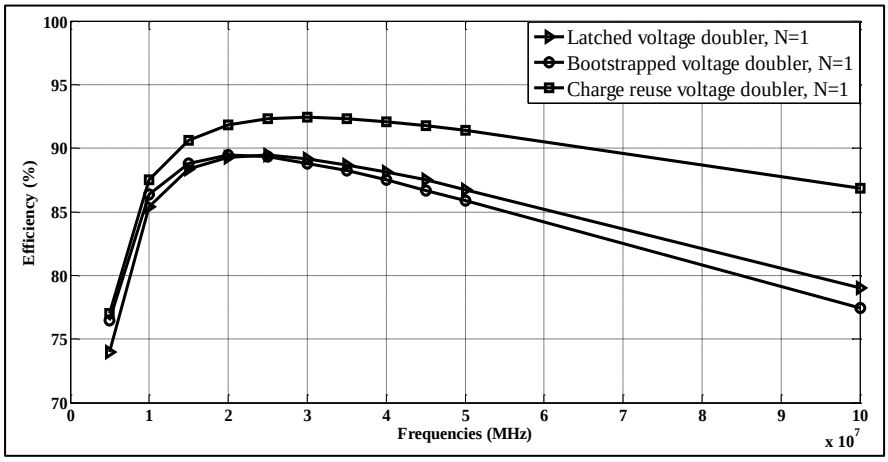

Fig. 15. Power efficiencies of a one stage latched, bootstrapped and charge reuse VD as a function of frequencies when I_o=1 mA, V_{DD} =3.5 V.

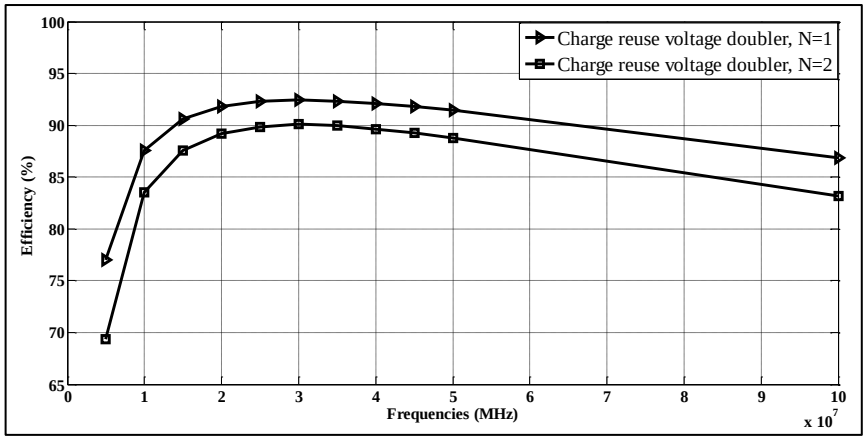

Fig. 16. Power efficiencies of a one stage and two stage for charge reuse voltage doubler as a function of frequencies when I_o=1 mA, V_{DD} =3.5 V.

5. Conclusions

Voltage doubler structure include one stage and two stage of a latched voltage doubler, bootstrapped voltage doubler and bootstrapped voltage doubler with charge reuse were designed and realization. The realization is based on CMOS 0.35-µm technology at supply voltage V_{DD}=3.5 V and input clock frequency f = 10 MHz. The design and analysis were in the time domain of the voltage doubler circuits were investigated at different operating frequencies and supply voltages. It was found that the VD charge pumps is suitable for operation of power IC, continuous time filters, EEPROM and switched-capacitor transformers in voltages higher than the power supplies are frequently required. The voltage doubler circuits were designed and simulated with OrCad 16.0 Cadence software. The charge reuse voltage doubler circuit provided a good efficiency about (87.6%) and (83.5%) for one stage and two stage respectively at pumping capacitance of 57 pf, loading current of 1 mA, clock frequency of 10 MHz and supply voltage is 3.5 V compared with one stage and two stage of a latched voltage doubler are (85.4%) and (80%) respectively. As well as, charge reuse method showed good output voltages with respect to latched VD circuit.

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