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PERFORMANCE ANALYSIS OF POWER GATING TECHNIQUES IN 4-BIT SISO SHIFT REGISTER CIRCUITS

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Abstract

The last few years have witnessed great deal of research activities in the area of reversible logic; the intrinsic functionality to reduce the power dissipation that has been the main requirement in the low power digital circuit design has garnered more attraction to this field. In this paper various power gating techniques for power minimization in adder and 4 bit serial in serial out (SISO) shift register circuits is proposed. The work also analyze various leakage reduction approaches such as sleep approach, sleepy stack approach, dual sleep technique and zig-zag technique for gate diffusion input technique, self resetting gate diffusion input technique for complementary metal oxide semi conductor (CMOS) technology and forced stack and multiplexer based SISO registers. A 4 bit SISO and full adder was designed in a cadence virtuoso 180 nm technology and the simulated results show the trade-off between power, delay and power for the sequential circuits and the results demonstrate that minimum power consumption can be achieved when the adder and SISO are designed for clock gating.

Keywords: Power gating, GDI, CMOS, SISO, Adder, Delay.

1. Introduction

A specific task considered here is to find ways to optimize the power savings of combinational and sequential circuits in the low power VLSI design. The energy consumption and feature size prediction of MOS transistors has become an emerging concern in today's nanometre technology in VLSI. The dynamic power reduction is done by using various methods. In low power applications, reducing the operating voltage is a better choice to lower switching power dissipation. The

Nomenclatures

L	Channel length, nm
uW	Power dissipation, watts
W	Channel width, nm

Abbreviations

D	Delay
DNA	Deoxyribonucleic Acid
CMOS	Complementary Metal Oxide Semiconductor
GDI	Gate Diffusion Input
FET	Field Effect Transistor
MOS	Metal Oxide Semiconductor
VLSI	Very Large Scale Integration
n-MOS	N Channel Metal Oxide Semiconductor

basic factors of leakage currents are reverse bias diode leakage and sub threshold leakage currents. The leakage current of the diode is proportional to the diffusions regions of source and drain terminals and reverse saturation current per unit area. The sub threshold current depends on applied gate to source voltage. The energy consumption, saving is achieved by incorporating power gating techniques in the functional units of processor like an adder and register circuits [1].

The leakage control transistor is used to increase energy saving from 40% to 90% over conventional technique [1]. The sleep method is used to control the leakage power when it is in ON mode of operation [2]. The zig-zag approach minimizes the wake up time caused by leakage control transistors [3, 4]. Another method for controlling reverse saturation current is the stack approach, which forces a series transistor by breaking down an available transistor into minimum size transistor [5]. The sleepy stack approach combines the features of sleep and stack techniques [6].

The basic block of the shift register is delay flip-flop. The serial in serial out register is designed by cascading four delay flip flops. The D flip flop is designed using many techniques named as multiplexer, gate diffusion input technique, and self resetting gate diffusion input technique and forced stack technique [7-9]. The full adder is an essential component of filter banks and it is used for biomedical applications. The various power gating techniques are addressed for energy saving in system and functional units like an adder and shift register circuits [10-14].

The circuit switches between active and drowsy mode and it is not suitable for long idle time due to maximum reverse bias current. This process is called as super buffer approach. In order to eliminate the problem in super buffer approach, the tri modal switch is introduced. The main concept of switch is to maintain the data by charge recycling process. To provide data stability and eliminate sneak path in the circuit is done by using low power multimodal switch. It is operated in three modes of operation namely, drowsy, sleep and active.

Multi threshold CMOS is efficient leakage reduction method that gives better energy consumption by function of both high and low threshold voltage transistor.

By applying variable body bias voltage from an enable circuitry to the lowest leakage current is achieved by applying variable body bias voltage from an enable

circuitry. This technique is called as variable threshold CMOS technique. The footprint of the chip is increased due to control circuitry.

The energy saving is achieved by percentage of leakage reduction in circuit. They are several techniques are used for leakage reduction in transistors. The input vector control is used for indentifying the control line of the circuit and maximizes the off transistors in the circuit due to stack effect. Another method is to test all input patterns to get the test vectors with the minimum leakage current. The substrate and gate of all the transistors are tied together. During idle time the leakage is low and run time the leakage is more. This technique is called as dynamic threshold MOS. In microprocessor system consists of data path and memory systems. The basic idea is to shut down power supply for idle systems. This is done by using high threshold transistors.

This paper is organized as follows: section 2 deals with various power gating techniques for low power VLSI. Section 3 discusses about the implementation of 4 bit serial in serial out shift register and multiplexer based, full adder circuits with power gating techniques. Section 4 analyzes the simulation results and measuring power, delay and power delay product using cadence virtuoso software. Section 5 concludes the remarks about clock gating techniques in low power circuits.

2. Power Gating Techniques

The sleep method consists of logic block and two extra transistors named as header and footer transistors. The true and complementary signals are fed to header and footer transistors. When the control signal is true both header and footer transistors are in closed switch, then it performs normal operation. The sleep method controls the leakage power during off mode. The power gating using the sleep method is shown in Fig. 1.

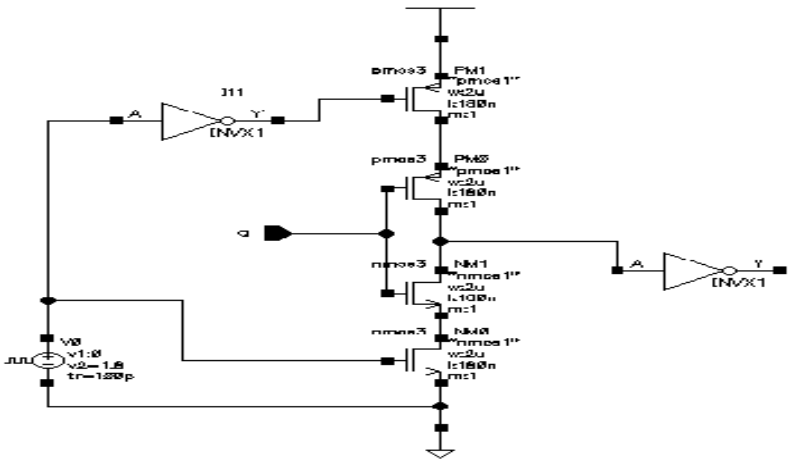

Fig. 1. Sleep technique.

The basic concept of sleepy stacks technique is to control the leakage power by combining the active mode of sleep transistor and sleep mode of stack transistor.

The sleepy stack technique consists of the parallel combination of p-MOS transistor and n-MOS transistor. So the area requirement of sleepy stacks technique is more when compared to sleep technique. The stacked transistors are used to reduce the sub threshold current in sleepy stack technique is shown in Fig. 2.

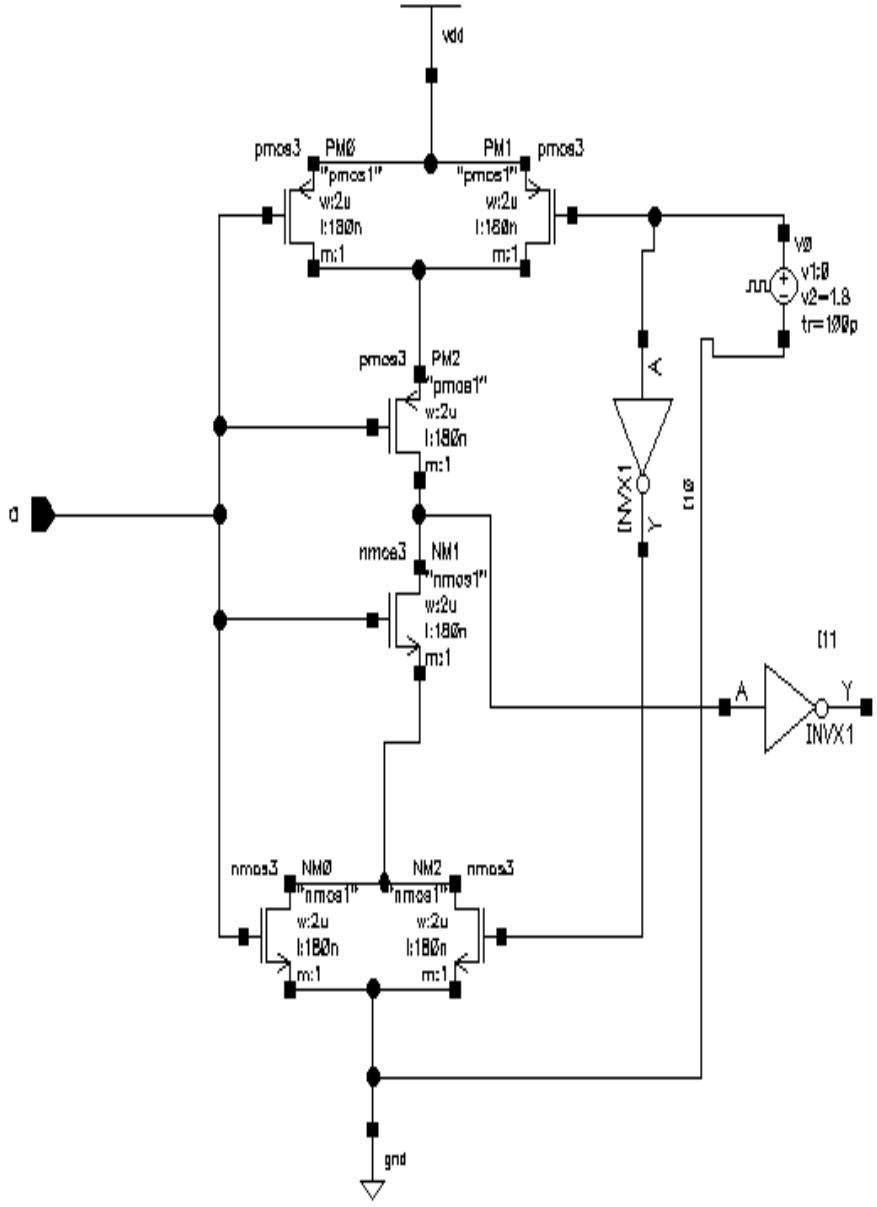

Fig. 2. Sleep stack technique.

Dual sleep technique consists of true and complements signals feeding into a pair of n-MOS and p-MOS in header and footer transistors. The dual sleep technique uses one more leakage control transistor than sleep technique in the

footer and header area. So the area requirement is more comparable to sleepy stack technique. The dual sleep technique is shown in Fig. 3.

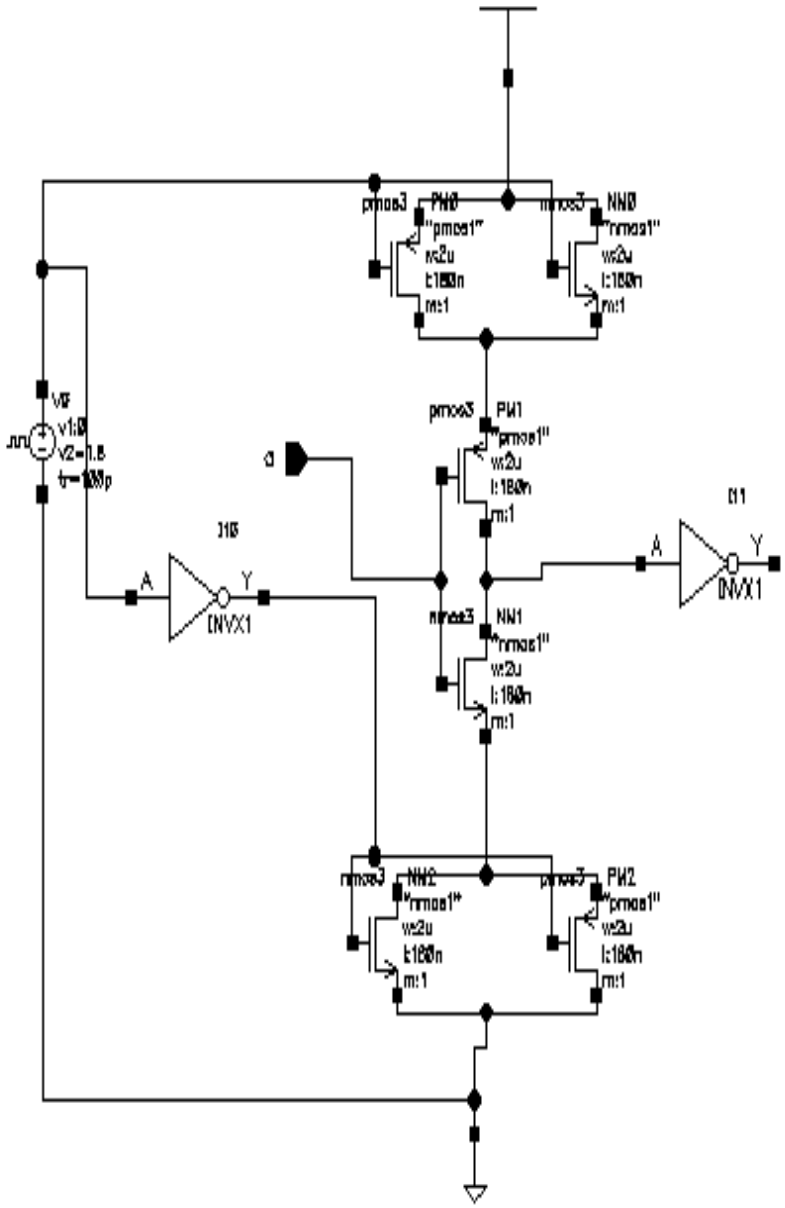

Fig. 3. Dual sleep technique.

The zig-zag technique uses a minimum number of leakage control transistors than sleep technique. In zig-zag approach, the complementary and true signals are inserted alternately between header and footer transistors. These header and footer transistors are acting as control transistor to minimize the energy saving and it is

mainly used for minimizing the wake up time. Therefore, we apply a footer leakage control transistor for the first block and a header leakage control transistor for second block. The diagram of zig-zag approach is shown in Fig. 4.

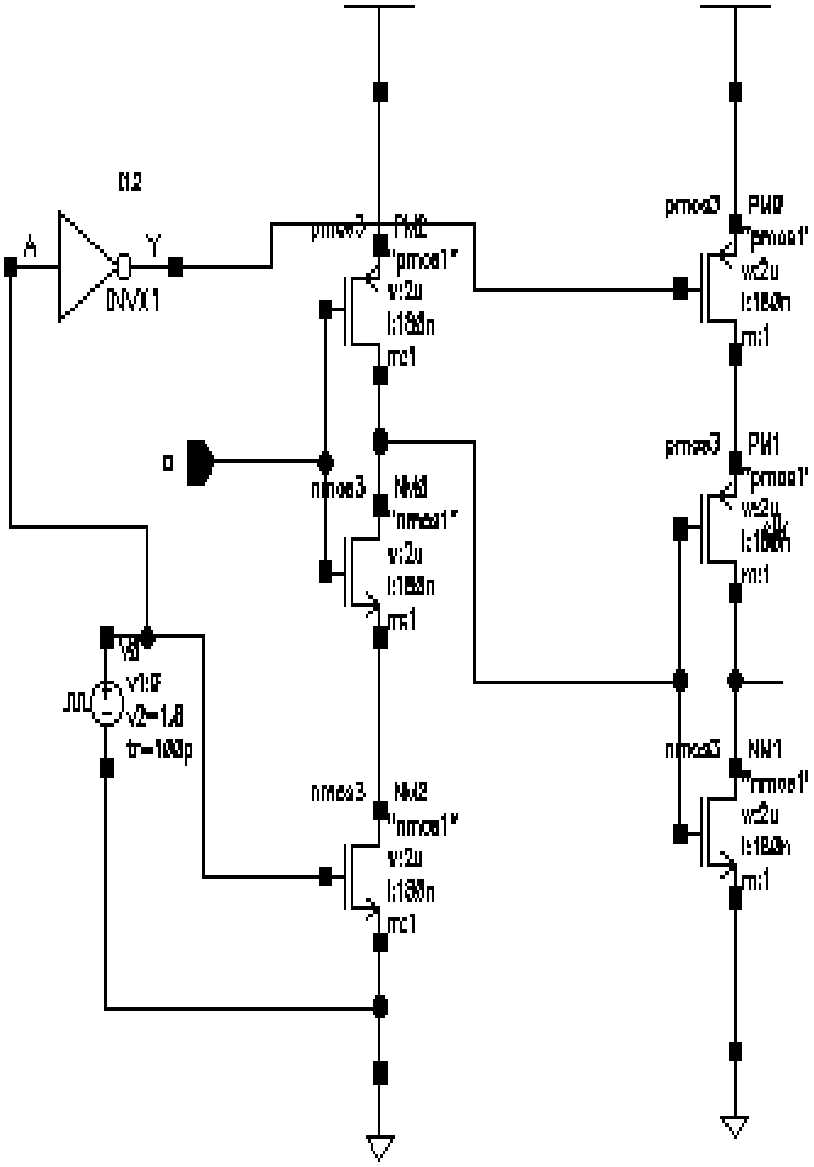

Fig. 4. Zig-zag technique.

3. Analysis of Shift Registers Using Power Gating Techniques

The basic module used for serial in serial out shift register is D flip-flop. It is the basic cell to store information as 0 or 1. The D flip-flop is realized by using two 2:1 multiplexers. The true and complementary clock signals are applied to multiplexer 1 and multiplexer 2 blocks respectively. When a clock is enabled and

input is one, and then we will get output as one otherwise the output is zero. The schematic diagram of a D flip-flop using multiplexer is shown in Fig. 5.

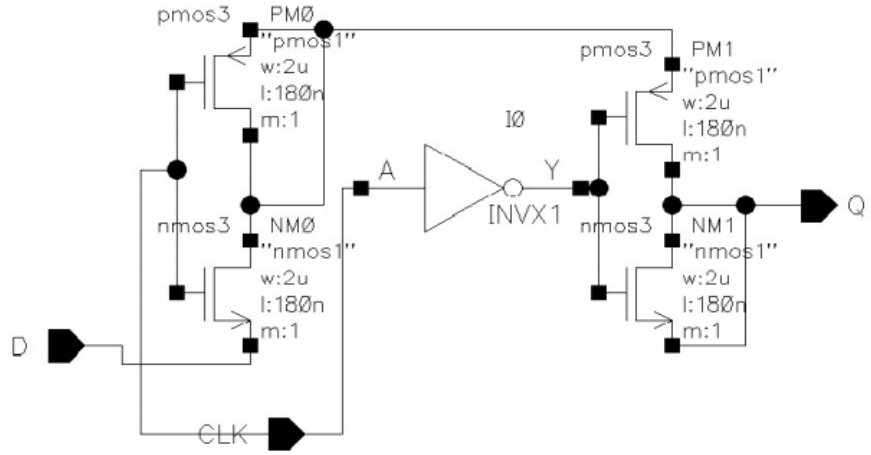

Fig. 5. D storage element with multiplexers.

When the clock transition is from 0 to 1, master responds for storing the information and when the clock transition is from 1 to 0 slaves responds to hold the value until clock changes from 0 to 1. The conventional D flip-flop is shown in Fig. 6.

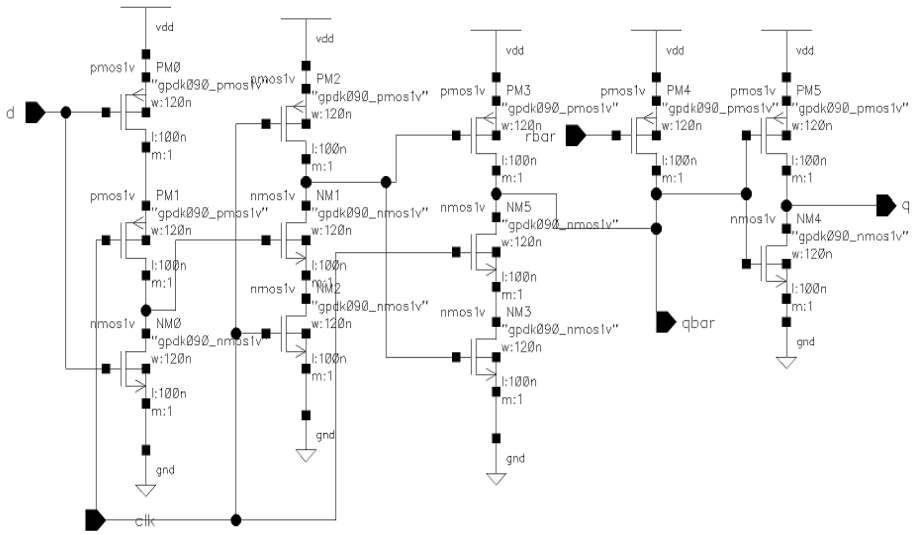

Fig. 6. D storage element using conventional technique.

The power consumption of the shift register is developed by using GDI technique. The proposed D storage element consists of two D latches. The implementation of

D flip-flop using GDI technique is shown in Fig. 7.

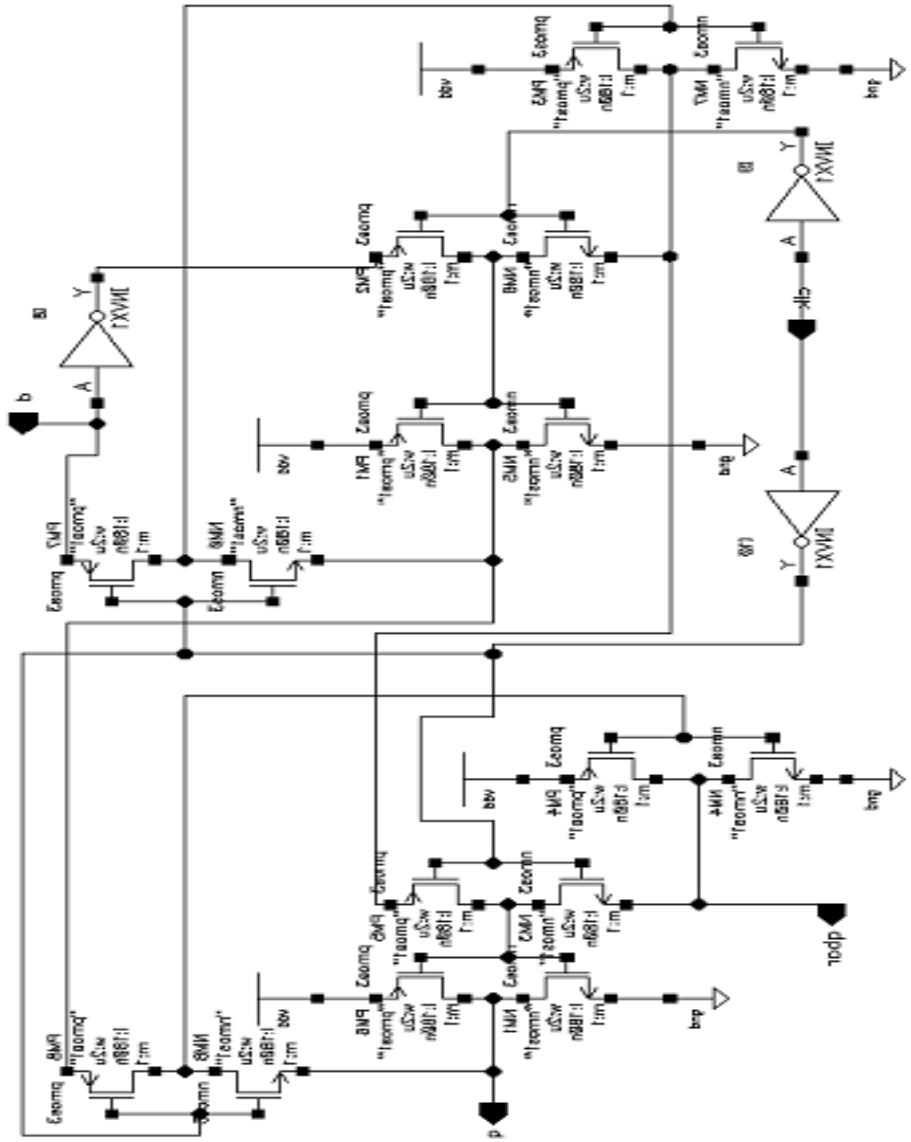

Fig. 7. D storage element using GDI technique.

In self resetting, GDI further improves the performance of D flip-flop and uses a level restoration technique. It provides both true and complementary outputs. Each circuit consists of GDI and resetting logic circuits. The schematic diagram of self resetting GDI logic is shown in Fig. 8.

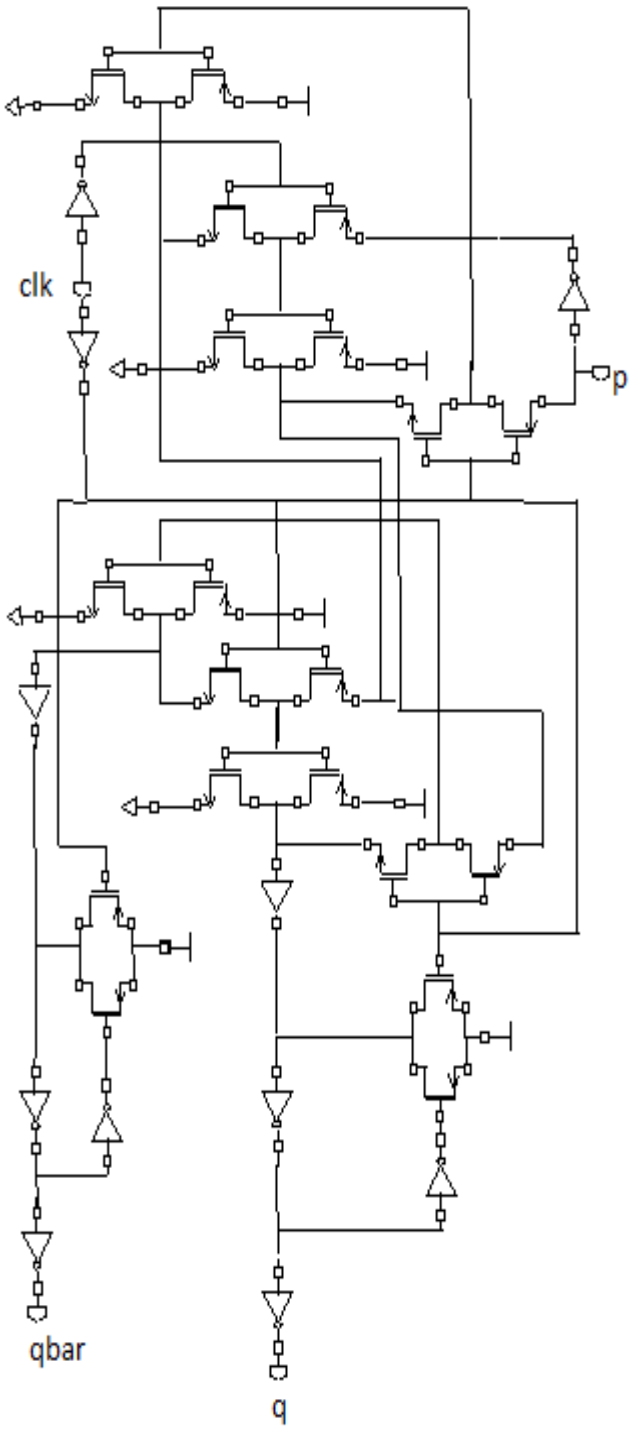

Fig. 8. D flip-flop using self resetting logic GDI technique.

4. Results and Discussion

To show the analysis of energy consumption in power gating design, choose generic circuit as 4 bit serial in serial out shift register. The sizing of each design, choose W/L = 2 µ / 180 n for p-MOS and n-MOS respectively. In each analysis, the supply voltage is chosen as 1.8 V in 180 nanometre technology and run all the simulation results with input patterns at room temperature of 300 K. The maximum frequency rate is 25 MHz and measure the average power consumption and delay of all the techniques in the shift register using transient analysis.

The switching power is calculated with an input pattern using Monte Carlo simulation for every clock pulse of the circuit. The propagation delay is estimated as the average sum of the delay occurs in switching transition from 0 to 1 and 1 to 0.The energy consumption is calculated by using the values of power and delay of the appropriate circuit. In order to implement serial in serial out shift register, create a test bench circuit of D flip-flop, supply voltage is set at 1.8 V and the performance of D flip-flop is analyzed in terms of power and delay.

Table 1 shows simulation results of D flip-flop using various techniques. The D flip-flop using GDI technique consumes less power and CMOS technique reports least delay when compared to all other techniques. Table 2 reports the 4 bit serial in serial out shift register using the gate diffusion input technique, multiplexer and self resetting GDI technique. The multiplexer based 4 bit serial in serial out shift register shows 50.03% reduction in power consumption and 83.36% reduction in delay compared to GDI and self resetting GDI techniques as shown in Table 4. Simulation results for gate diffusion based input technique based 4 bit serial in serial out shift register using various power gating techniques as shown in Table 3. The zigzag power gating technique has achieved a 22.37 % reduction in power consumption when compared to sleepy stack and dual sleep technique. The dual sleep technique produces least delay when compared to sleep, sleepy stack and dual sleep technique. In order to incorporate various power gating techniques in self resetting GDI based 4 bit serial in serial out shift register as reported in Table 5..The sleep techniques consume low power compare to all power gating techniques. It brings 14.21 %, 8.8%, 6.2% reduction in power consumption for the techniques, dual sleep, sleepy stack and zigzag technique. The dual sleep technique produces low delay compare to sleep, sleepy stack and zigzag.

Table 1. Simulation results for D flip-flop in 180nm technology with 1.8 V supply.

Technique	Delay	Power
Gate diffusion input	43.35 ns	200.3 uW
CMOS	134.45 ps	89.0 uW
MUX	987.00 ps	84.89 uW
Self resetting logic GDI	43.26 ns	1.506 mW

Table 2. Simulation results for serial in serial out shift register without power gating techniques in 180nm technology with 1.8 V supply.

Technique	Delay	Power
Gate diffusion input	49.20 ns	751.8 uW
MUX	327.01 ns	370.4 uW
Self resetting logic GDI	1125.57 ns	7.291 mW

Table 3. Simulation results for gate diffution input based SISO register using power gating techniques in 180 nm technology with 1.8 V supply.

Technique	Delay	Power
Zig-zag	89.92 ns	459.4 uW
Sleep	429.03 ps	555.9 uW
Sleepy	388.07 ps	652.6 uW
Dual sleep	374.05 ns	653.3 uW

Table 4. Simulation results for multiplexer based SISO register using power gating techniques in 180 nm technology with 1.8 V supply.

Technique	Delay	Power
Zig-zag	4.967 ns	233.0 uW
Sleep	79.45 ns	253.0 uW
Sleepy	4.88 ns	279.0 uW
Dual sleep	4.92 ns	236.5 uW

Table 5. Simulation results for self resetting GDI based SISO register using power gating techniques in 180 nm technology with 1.8 V supply.

Technique	Delay	Power
Zig-zag	54.54 ns	6.651 mW
Sleep	20.31ns	6.235 mW
Sleepy	207.69 ps	6.841 mW
Dual sleep	207.61 ps	7.268 mW

5. Conclusions

In this paper, 4 bit SISO register circuits based on the power gating techniques have been presented. It observes from the transient results power gating techniques reduce power up to 20 % when compared to conventional techniques. As apply the zig-zag technique, observe 74.39% reduction in power consumption than dual sleep technique and finally conclude that in many cases zig-zag based power clock gating is a better choice for sequential circuits.

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