

# SEU Rate in 90nm and 180nm of 6T SRAM at NEqO Orbit

Ooi ST<sup>1</sup>, Souaad Benkara<sup>2</sup>, Sharizal Fadlie Sabri<sup>1</sup> and Nurul Fadzlin Hasbullah<sup>2</sup>

<sup>1</sup>Development & Operational Space System Division, National Space Agency, 42700 Banting, Selangor, Malaysia.

<sup>2</sup>Electrical & Computer Engineering, International Islamic University Malaysia, 53100 Kuala Lumpur, Malaysia.  
stooi@angkasa.gov.my

**Abstract**—RazakSat® was a remote sensing satellite which functioned as to acquire the information from the earth surface. RazakSat® was launched to low altitudes, around 600km above the earth surface in 2009. Although RazakSat® was a low altitude satellite but the malfunction of the RazakSat® was suspected experienced high rates of anomalies. The main factor of getting high rates of anomalies is due to the RazakSat® was exposed to space radiation environment when the satellite passed through the South Atlantic region at its NEqO trajectory. An investigation was carried out to predict the Single Event Upset (SEU) rate for 6T SRAM, which is located at On-Board Computer (OBC) of the satellite. The results show that the Q node in 6T SRAM is the most sensitive node and this node becomes the main focus in this paper in order to estimate direct ionisation induced SEU rates in the worst case scenario. Apart from that, the comparison by using 90nm and 180nm of 6T SRAM are shown whereby with 90nm, around 1083.5 error/bit day is occurred and there is around 4.538 errors/bit day is found by using 180nm of the 6T SRAM.

**Index Terms**—RazakSAT; Single Event Upset (SEU); Near Equatorial Orbit (NEqO); On-Board Computer (OBC); Ionization.

## I. INTRODUCTION

Malaysia is the first country to place the satellite into Near Equatorial Orbit (NEqO) during the launch of RazakSAT® on 14 July 2009. The use of NEqO offers imaging opportunity and more communication window for areas at or near to equator. The previous RazakSAT® records showed that RazakSAT® can provide more than 11 passes per day and it takes about 16-17 minutes to communicate with ground station located at Banting, Malaysia. With these advantages, it is believed that placing a satellite at NEqO could overcome the long-existing problem, heavy cloud coverage that will deteriorate the quality of the image taken by satellite for countries located at or near equator region.

Unfortunately, the RazakSAT® was only able to operate for nearly a year. It is believed that one of the factors was due to space radiation environment experienced by RazakSAT® when it passed through NEqO trajectory and leading to malfunction of the SRAM at its OBC. In NEqO trajectory, there is a region where the low altitude satellites are in vulnerable position when exposed to radiation hazards resulting from solar emissions and cosmic rays [1,2]. This region is spanning the southern Atlantic and South America where an apparent local depression of the Earth's magnetic field is observed and it is also known as South Atlantic Anomaly (SAA). In the term of astronomy, the tilting angle takes about 11 degree for the magnetic axes of the Earth

relative to the rotation axes of the earth cause one of the equatorial region in NEqO trajectory, South America are exposed to South Atlantic Anomaly(SAA), as shown in figure 1. SAA is characterized as high radiation region as the inner radiation Van Allen belt reaches the lowest altitudes of 200km where particles in the inner radiation belt reach their highest intensities. [3,4,5] Those satellites will experience high rates of anomalies when pass through this region [6]. The failure of the Globalstar and RazakSAT® are thought to be caused by this reason although they are in low altitudes.

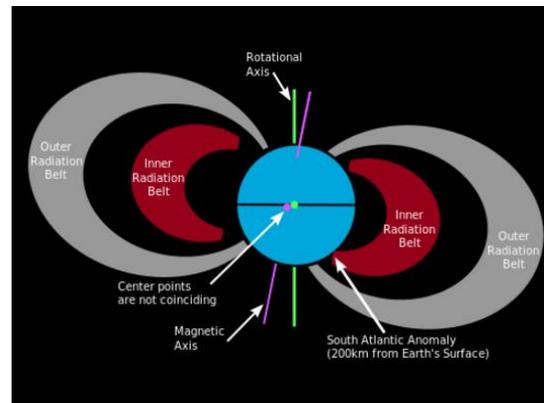


Figure 1: Due to axial tilting of the earth, the inner radiation belt reaches the altitudes of 200km from Earth's surface over the South Atlantic ocean.[2]

The paper is organized into four (4) sections: the first section presents an introduction which regards to the benefits of utilizing NEqO and the failure suspected happened at RazakSAT® that was launched into NEqO space environment. The second section provides a literature review satellite's memory like SRAM based FPGA and its Single Event Upset (SEU) while the third section describes the methodology of the project. The forth section details the results and discussions of the simulation works that have completed and the final section summarizes the important points derived from the project.

## II. LITERATURE REVIEW

Radiation has high Linear Energy Transfer (LET) value and remarkable effect on satellite's memory. To investigate the radiation effect on satellite's memory it is important to understand the structure of 6T SRAM (Static Random Access Memory) and the SEU effect happened on it.

A. Static Random Access Memory (SRAM)

SRAM is a memory element that is a key part of the core of many systems. Most high-performance systems have SRAMs with them. Nearly all SRAMs either use a 4-transistor or a 6-transistor Memory Cell. These cell structures allow data to be stored for an indefinite amount of time in the device as long as it is powered. However, our study is only focuses on the 6-transistor cell SRAMs (usually referred to as 6T cells). The SRAM cell is formed by two cross-coupled inverters and two access transistors, as can be seen in Figure 2.

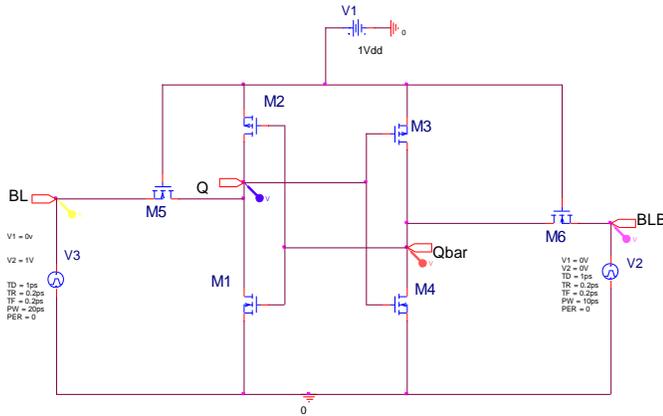


Figure 2: Transistor memory cell (6T Cell) in ORCAD PSPICE

Access transistors in SRAM cell is enabled by word line (WL). Once the WL is enabled, access transistors could transfer data in both read and write operations as they connect with the bit line (BL) or bit line bar (BLB). BL and BLB serve to control access to a storage cell during read and write operations in 6T SRAM. This storage cell has two stable states, which are used to denote 0 and 1.

Write operation is writing a bit into the SRAM cell is done by forcing one of the bit lines high while keeping the other low. To write “1” into the SRAM cell the word line (WL) is asserted bit line BL is made high and bit line BLB is made low. To write “0” into the SRAM bit line BL is made low and BLB is made high [7]. For read operation, both bit lines are pre-charged close to supply voltage before reading from SRAM cell. WL will select a particular cell to be read and then charge stored at node discharges of that particular cell will be discharged through BL and BLB. BL of particular cell acts as input to sense amplifier in order to sense amplifiers and then amplifies the difference of the data. It happened to voltage difference between BL and BLB If voltage at BL < BLB output amplify to logic 0 else if voltage at BL > BLB output amplify to logic 1 [7].

B. Single Event Upset (SEU) in SRAM

The cross-coupled inverters are highly asymmetric with the pull-down NMOS transistors and having much stronger drive strength than the PMOS pull-ups. The following figure illustrates the two cross-coupled inverters and the pulse current injected at the drain of the off NMOS in a simulated circuit showed in figure 3. Generally, in CMOS SRAM circuits, the transistor is ‘off’ as they are stroked by heavy ions with high enough Linear Energy Transfer (LET) in the junction area, experience single event upset (SEU) [8,9] as it is shown in

(Figure 4). When the SEU occurs, the minority carriers are created and collected by the source drain diffusion regions cause a change in the nodes voltage value occurs. The cross-coupled inverters are highly asymmetric with the pull-down NMOS transistors and having much stronger drive strength than the PMOS pull-ups. The following figure illustrates the two cross-coupled inverters and the pulse current injected at the drain of the off NMOS in a simulated circuit showed in figure 3. Generally, in CMOS SRAM circuits, the transistor is ‘off’ as they are stroked by heavy ions with high enough Linear Energy Transfer (LET) in the junction area, experience single event upset (SEU) [8,9] as it is shown in (Figure 4). When the SEU occurs, the minority carriers are created and collected by the source drain diffusion regions cause a change in the nodes voltage value occurs.

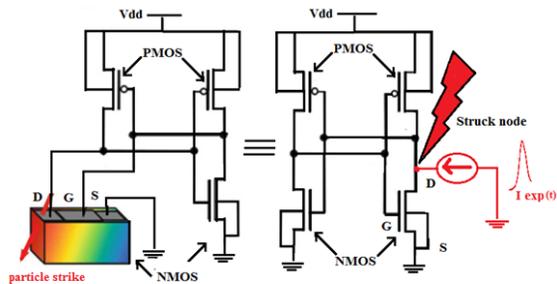


Figure 3: The pulse current injected at the drain of the off NMOS

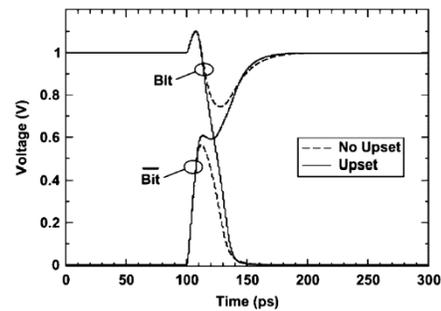


Figure 4: The graph with and without upset experienced by the transistor [9]

C. The Critical Charge for SEU Inducement

The minority carriers are created and collected by the source drain diffusion regions when they hit the silicon bulk. Followed by this, the induced transient voltage pulse propagates through several logic gates and cause a change in the nodes voltage value occurs. Either the drain region of an off NMOS transistor or an off PMOS transistor is considered as sensitive areas. The collected charge at either of this sensitive nod is compared with the minimum charge that could cause an upset of the device. This minimum charge is called critical charge (Qcrit). The simplest approach for Qcrit calculation is to consider it as the sum of capacitance and conduction components. The formula of Qcrit is as follows [10]:

$$Q_{crit} = CNVDD + IDP TF \tag{1}$$

where: CN = the equivalent capacitance of the struck node;  
 VDD = the supply voltage;  
 IDP = the maximum current of the ON PMOS or  
 NMOS transistor; and  
 TF = the cell flipping time.

### III. METHODOLOGY

Principally, two simulation packages are used: ORCAD PSPICE version 9.2 and Space Environment Information System (SPENVIS). The PSPICE software is used to generate two types of the circuit model of the 6T-SRAM in 90nm and 180nm to compute the critical charge caused by radiation that induces SEUs accurately. Once the critical charge is obtained by using ORCAD PSPICE, the results will be further correlate with Space Environment Information System (SPENVIS) by developing various incorporated space radiation environment models specifically in SEUs.

#### A. ORCAD PSPICE Version 9.2

A 90nm and 180nm of 6T SRAM cell models which consist of IBM transistors are simulated in order to compare the critical charge ( $Q_{crit}$ ) among these two models. Both models are adopted with the same method which is, an exponential current is injected incrementally at a nominal supply voltage ( $V_{dd}$ ) until the cell state is flipped. After that,  $Q_{crit}$  could be computed by integrating the injected current up to the flipping time. By observing the  $Q_{crit}$ , the transistor sizes in SRAM circuit are optimized to ensure reading operation stability. Figure 5 summarises the steps to obtain the  $Q_{crit}$ .

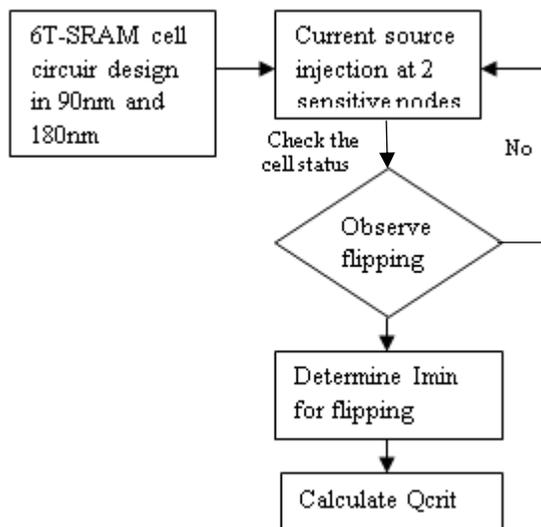


Figure 5: The methodology by using ORCAD PSPICE

#### B. Space Environment Information System (SPENVIS)

Space Environment Information System (SPENVIS) incorporates several models to describe the space environment and its effect upon various materials [11]. The focus of the project is to investigate the SEU rate at NEqO orbit and hence all parameters which regards to NEqO orbit are set in every types of simulation model (Table 1). The various types of simulation model that suits to various ion energy spectra are determined (Table 2) in order to derive the SEUs rates produced

by trapped particles, solar particles and galactic cosmic ray environment.

Table 1  
Parameters are set in all various simulation models

Num.	Parameter	Value
1	Inclination	8.99°
2	Apogee	706.39km
3	Perigee	664.65km
4	True Anomaly	337.07°
5	Right Ascension of Ascending Node	350.85°
6	Eccentricity	0
7	Argument of Perigee	22.93°

Table 2  
Various SPENVIS radiation models are selected for respective radiation

Num.	Types of Radiation	SPENVIS Radiation Model
1	Trapped Proton	AP8
2	Trapped Electron	AE8
3	Solar ParticlesEvent	CRÈME96 SPE
4	Galactic Cosmic Rays	ISO 15390

### IV. RESULTS AND DISCUSSIONS

Owing to the intensified competitive pressure and necessity for entering to global market undergone by electronic companies to account for technological advancement and competitive advantages, it is noticeable that the smaller size of embedded technology is widely adopted. [12,13] Thus, the main objectives of the project is to make comparison between 90nm and 180nm of the 6T SRAM in order to know the sustainable level particularly the occurrence of SEU. To meet the objectives of the project, there is several scenario simulation models are developed as follows;

1. Comparison between the sensitivity of Q and  $\bar{Q}$  node in 90nm and 180nm of the 6T SRAM;
2. Current injection at Q node in 90nm of the 6T SRAM;
3. Current injection at Q node in 180nm of the 6T SRAM;
4. SEU rate at Q node in 90nm of 6T SRAM at NEqO orbit;
5. SEU rate at Q node in 180nm of 6T SRAM at NEqO orbit.

#### A. Comparison between the sensitivity of Q and $\bar{Q}$ node in 90nm and 180nm of the 6T SRAM

The current is injected to the sensitive node, Q and  $\bar{Q}$  node in SRAM in order to know the minimum of charge  $Q_{crit}$  that cause upset. In this case, a comparison in term of its sensitivity is analysed between Q and  $\bar{Q}$  node. Then the analysis on most sensitivity node is furthered with several of the investigations to take into account as a worst case scenario which regards to this paper. Figure 6 and 7 shows that the most sensitive node is Q node as it is able to sense the minimum charge of 0.18fC whereby  $\bar{Q}$  node sense the minimum 0.36fC in 90nm and 180nm of the 6T SRAM.

#### B. Current injection at Q node in 90nm of the 6T SRAM

Next, the current is injected into the Q node in order to observe the occurrence of the upset happened in SRAM. Figure 8 shows the injected current of 0.46mA whereas Figure 9 shows the injected current is 0.47mA. The upset is occurred when the injected current is 0.47mA in 90nm of the 6T SRAM

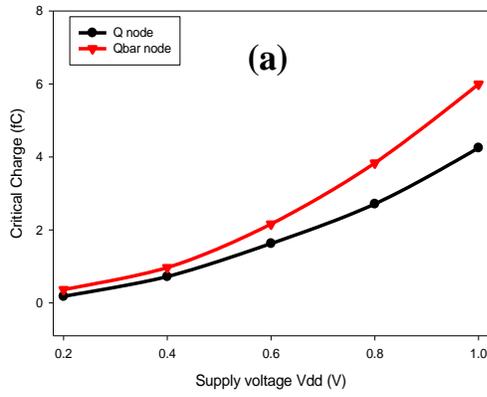


Figure 6: The minimum of charge that able to sense by Q and its  $\bar{Q}$  node in 6T SRAM in 90nm

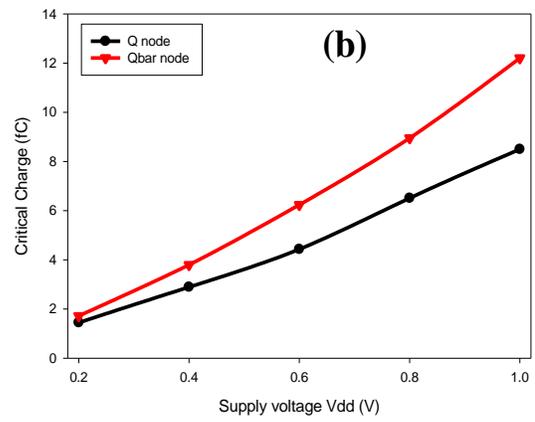


Figure 7: The minimum of charge that able to sense by Q and its  $\bar{Q}$  node in 6T SRAM in 180nm



Figure 8: No upset is occurred when the injected current is 0.46mA

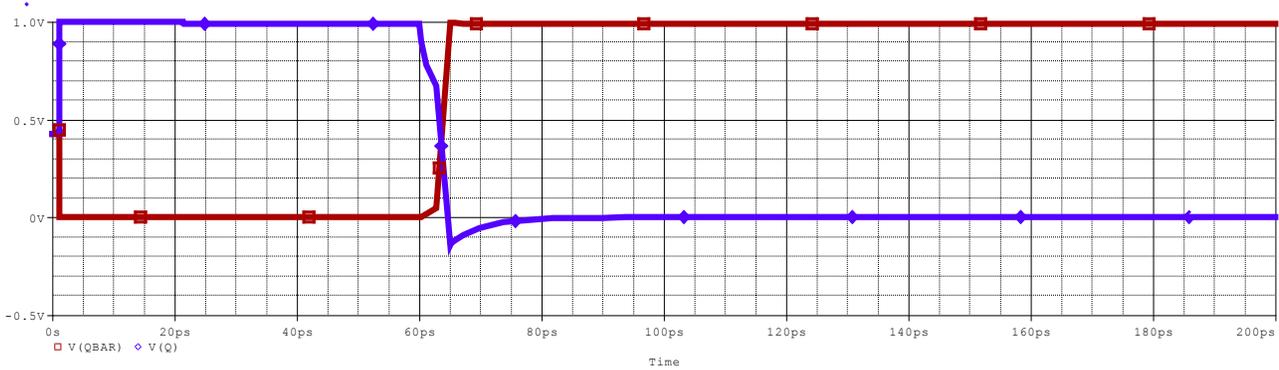


Figure 9: Upset is occurred when the injected current is 0.47mA

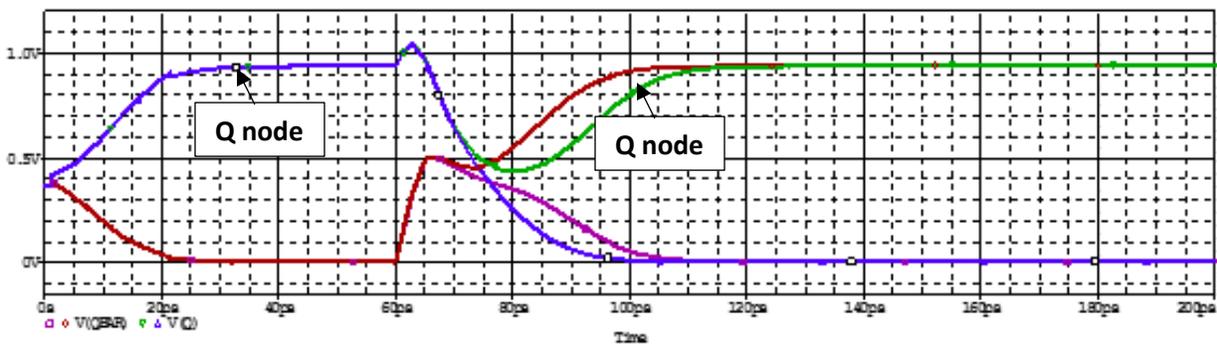


Figure 10: No upset is occurred when the injected current is 1.34mA (green colour) whereby upset is occurred when the injected current is 1.35mA (cyan colour)

C. Current injection at Q node in 180nm of the 6T SRAM

From Figure 10, it is noticed that there is no upset is occurred when the injected current is 1.34mA (in green colour) and the upset is occurred when the injected current is 1.35mA (in cyan colour) in 180nm of the 6T SRAM.

D. SEU rate at Q node in 90nm of 6T SRAM at NEqO orbit

Before proceed to SPENVIS simulation model, one more graph is generated in order to relate the injected current and the critical charge. The results obtained prior to this are used to apply into SPENVIS in order to perform further analysis in NEqO orbit. Referring to Figure 11, it shows that the injected current 0.47mA could induce ~ 4.2fC. Figure 12 provides direct ionization SEUs rates at NEqO orbit concerning a minimum of 3 years lifetime of a satellite. Within these 3 years, a satellite experiences particles environment consists of solar protons, trapped protons and GCR particles at NEqO. In Figure 12, it is observed that the densely shaded region of upsets is homogeneously spread all over the orbit, where the SEU rates are around 1083.5 errors/bitday.

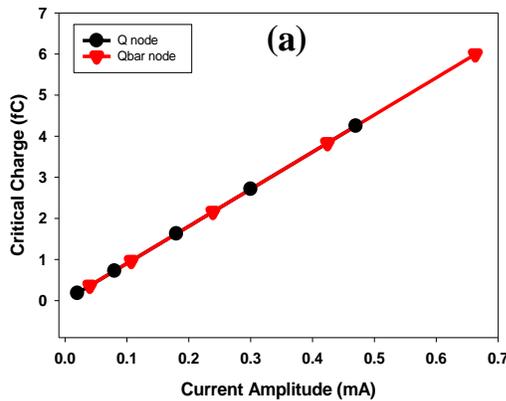


Figure 11: The critical charge as a function of injected current resulted from particle strikes at Q node in 90nm

from the simulation, it is proved that the flipped bits are less occurs when using 180nm of 6T SRAM appearance in the text.

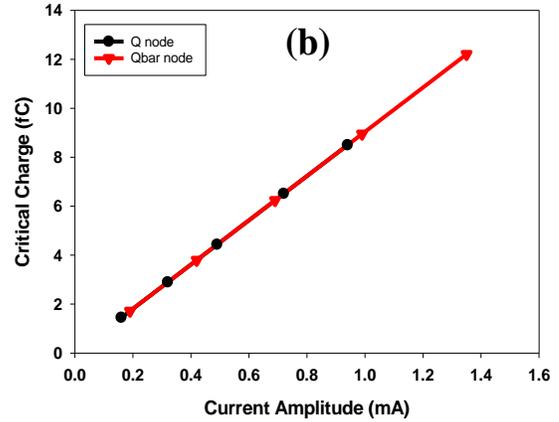


Figure 13: The critical charge as a function of injected current resulted from particle strikes at Q node in 180nm

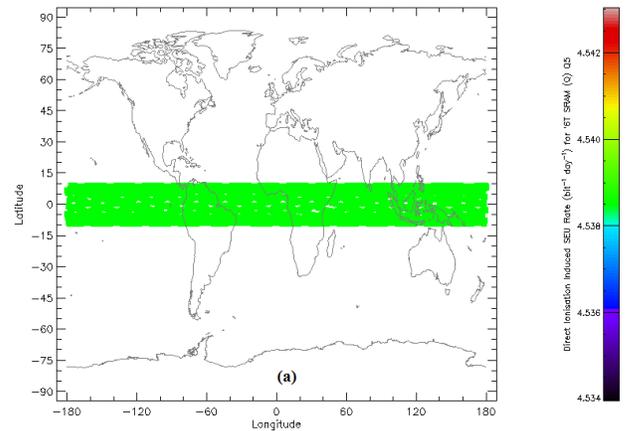


Figure 14: Direct ionization SEUs rates concerning NEqO orbit in 3 years lifetime mission in 180nm

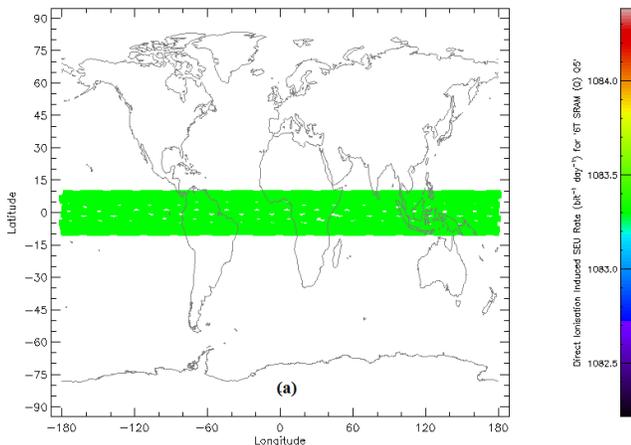


Figure 12: Direct ionization SEUs rates concerning NEqO orbit in 3 years lifetime mission in 90nm.

E. SEU rate at Q node in 180nm of 6T SRAM at NEqO orbit

In figure 13, it shows that the injected current 1.35mA could induce ~ 12fC whereby figure 14 shows the direct ionization SEUs rates obtained is ~ 4.538 errors/bitday at NEqO orbit in 3 years lifetime of a satellite. Referring to the all results obtained

V. CONCLUSION

The paper has successfully performed an investigation on the critical charge, Q<sub>critic</sub> that cause upset to occur in 90nm and 180nm of 6T SRAM. Furthermore, the direct ionisation induced SEU rates in NEqO are also obtained in order to know the number of errors are occurred per bit –day.

In short, it is noticeable that the reduction of feature size in embedded system which cause the SEUs play an increasing role in failures observed during operation of digital circuits, particularly in space environments that exposed to a set of changing conditions which consist of magnetic fields, energetic particle radiation and others.

Therefore the counter measure against SEUs gains importance as nowadays consumer prefers using smaller size of technology.

ACKNOWLEDGMENT

This study is funded by Fundamental Research Grant Scheme (FRGS) with reference number FRGS/1/2014/TK03/MOSTI//1.

REFERENCES

- [1] R.Heitzler, The Future of the South Atlantic Anomaly And Implications for Radiation Damage in Space, *Journal of Atmospheric and Solar-Terrestrial Physics* 64, 1701–1708 (2002)
- [2] Hamilton. B, Macmillan. S, Beggan. C, Thomson. A, Turbitt. C, Predicting the South Atlantic Anomaly, *Magnetic Relaxation* (2012)
- [3] F.Javier Pavon-Carrasco, Angelo De Santis, The South Atlantic Anomaly: The Key for a Possible Geomagnetic Reversal, *Frontiers in Earth Science: Geomagnetism and Paleomagnetism* (2016)
- [4] Vernov S.N., Gorchakov E.V, Shavrin P.L., Sharvina K.N., *Terrestrial Corpuscular Radiation and Cosmic Rays, Space Science Revision* 7, 490-533 (1967)
- [5] Heitzler J.R, The Future of The South Atlantic Anomaly and Implications for Radiation Damage in Space, *Journal Atmosphere Solar Terrestrial Physics* 64, 1701-1708 (2002)
- [6] G.P. Ginet, D. Madden, B.K. Ditcher, D.H. Brautigam, *Energetic Proton Maps for the South Atlantic Anomaly, IEEE Radiation Effects Data Workshop*, pg 1-8 (2007)
- [7] Mohamed Abu Rahma, Mohab Anis, *Nanometer Variation-Tolerant SRAM: Circuits and Statistical Design for Yield*, pp.49-57 (2012)
- [8] J. S. Fu, C. L. Axness, and H. T. Weaver, *Memory SEU simulations using 2-D transport calculations, IEEE Electron.Device Lett.*, vol. 6, pp. 422–424, Aug (1985)
- [9] L. Anghel and M. Nicolaidis, *Cost reduction and evaluation of a temporary faults detecting technique, Design, Automation and Test in Europe Conference and Exhibition 2000*, pp. 591–598 (2000)
- [10] Jahinuzzaman, S. M., Sharifkhani, M., & Sachdev, M., *An analytical model for soft error critical charge of nanometric SRAMs. Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, 17(9), 1187-1195 (2009)
- [11] Murat Hudaverdi, Ilknur Baylakoglu, *Space Environment and Evaluation for RASAT, International Conference on Recent Advances in Space Technologies*, pg 926 – 931(2011)
- [12] K. Hirose et al., *SEU resistance in advanced SOI-SRAMs fabricated by commercial technology using a rad-hard circuit design, IEEE Transactions on Nuclear Science*, 49(6) (2002)
- [13] Gaurav Saxena, Rekha Agrawal, Sandhya Sharma, *Single Event Upset (SEU) in SRAM*, vol. 3(4), pp. 2171-2175(2013).