High Gain of 3.1-5.1 GHz CMOS Power Amplifier for Direct Sequence Ultra-Wideband Application

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***Abstract*—This paper presents the design a power amplifier (PA) for direct sequence ultra-wideband applications using 0.13 µm CMOS technology operating in a low band frequency of 3.1 GHz to 5.1 GHz. Current-reused technique is employed at the first stage to increase the gain at the upper end of the desired band. Cascaded common source configuration with shunt peaking inductor at the second stage helps to enhance the wideband frequency while increasing the gain approximately twice the performance. The simulation results specify that high gain of 20.3 dB with ± 0.8 dB flatness, group delay variation of ±121.3 ps, and good input return loss and output return loss is obtained over desired working band. The proposed PA achieves power consumption of 27.3 mW.**

***Index Terms*—Power Amplifier; Ultra-Wideband; CMOS; Techniques; Performance Criteria.**

I. INTRODUCTION

In recent year, many researchers involved in new technology i.e., ultra-wideband (UWB) system because of its capability to provide high data rate over short distance range as well as very low power consumption. Two UWB standards have been proposed by IEEE 802.15.3a, namely multiband orthogonal frequency division multiplexing (MB-OFDM) and direct-sequence code division multiple access (DS-CDMA) [1]. BPSK and bi-orthogonal keying (BOK) mode is used for DS-UWB to supports the data communication [2]-[3]. Figure 1 shows DS-UWB signal transmission with two important bands which are low band from 3.1-4.85 GHz and high band from 6.2-9.7 GHz. The advantages of DS-UWB are low cost, high efficiency that will lead to longer battery life, high data rate, robust and accurate spatial resolution for detecting the location.

Various CMOS PA designs for UWB application have been proposed with different techniques such as distributed amplifier [4]–[5], resistive shunt feedback [6]–[9], RLC matching [10], shunt-shunt feedback [11]–[12], shunt peaking [13], inductive source degeneration [14]–[15], current reuse [16]–[17], and stagger tuning [18]–[19]. Each of the technique offers different performance depending with PA specification design.

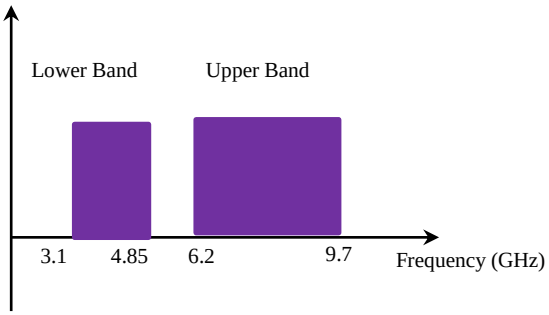

Figure 1: DS-UWB spectrum allocation

The distributed amplifier is commonly used for wide frequency range and can achieve good linearity. However, this technique consumes high power consumption and large chip area compared to other techniques due to the transmission line configuration used in this technique [4]–[5].

The RLC matching is the technique that needs a few reactive components to build RLC filter to provide good matching at the input and output for wideband application. The disadvantage of this technique is it produce large chip area because of a few reactive components is used for filter design [10].

Resistive shunt feedback is amongst popular technique that can offer very wideband matching at the input and output of the circuit [11]–[12]. This technique offers smaller chip area compared to other techniques since it is utilized no inductor or less inductors [20]. Current reuse is one of the topology which can provide low group delay and low power consumption. However, it is difficult to meet the requirement of high gain [16]–[17]. Another fabricated PA reported using stagger technique have shown that very wide band from 3.1 to 10.6 GHz, low group delay, high gain, good gain flatness and small chip area was implemented and designed in PA for UWB application [16]. However, this design consumes very high power consumption up to 100 mW and it is not suitable for UWB application.

In this paper, high gain of 3.1 GHz to 5.1 GHz UWB CMOS power amplifier by adopting current reuse technique is designed using 0.13 µm CMOS technology.

II. UWB PA DESIGN

Firstly, the design specification is established for proposed PA as shown in Table 1. This design specification is based on the target property for UWB applications that mentioned in [21].

Table 1
Proposed PA Design Specification

Parameter	Design Specification
Frequency (GHz)	3.1-5.1
Supply voltage (V)	1.8
CMOS technology (μm)	0.13
S_{21} (dB)	≥10 ± flatness (as low as possible)
S_{11} (dB)	≤ -10
S_{22} (dB)	≤ -10
Output impedance (Ω)	50
Stability	> 1
Power consumption (mW)	As low as possible
Group delay (ps)	As low as possible

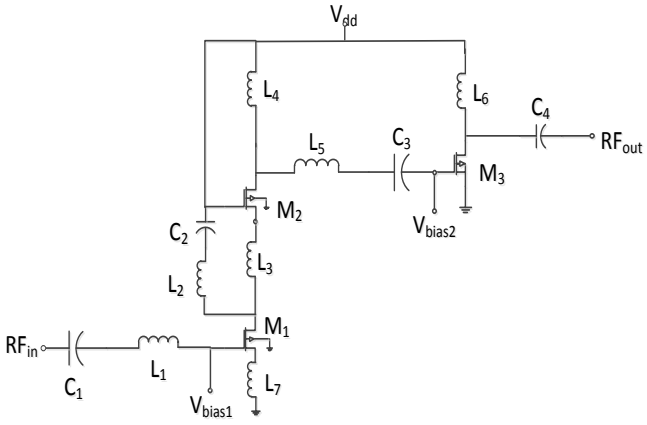

Figure 2: The schematic of the proposed DS-UWB CMOS PA

Then, the proposed CMOS PA is designed based on the design specification as shown in Table 2. Figure 2 shows the proposed design of the DS-UWB CMOS power amplifier which is divided into three stages. The first stage is known as current reuse technique where M_1 is common gate amplifier and M_2 is common source amplifier. The advantage of this current reuse technique compared to cascade technique, it can provide low power consumption that can be expressed in (1) and (2) [22].

$$P_{cascade} = 2V_{dd} \times I \quad (1)$$

$$P_{current-reused} = V_{dd} \times I \quad (2)$$

From Equation (1) and (2), the power consumption for cascade technique is twice power consumption of current reuse technique. Hence, the current reused technique is commonly employed to offer very low power consumption that suitable for UWB application. M_1 offers wideband input matching, input-output isolation and good linearity, however the PA gain power performance degrade at high frequency because of the existing of parasitic capacitance of transistor C_2. L_2 offers a low path impedance path of M_2 while L_3 with satisfactory large impedance is used to block the signal at the desired bandwidth. Thus, twice of the input signal can be produced using this technique for high gain approach [23]. In order to enhance the gain at upper end of desired bandwidth at 5.1 GHz, a narrow band characteristic composed by the resonate circuit of C_2 and L_2 is employed. L_4 is an inductive peaking to achieve high gain at high frequency. L_7 is shunt peaking for the flatness of the gain. Capacitor, C_1 and inductor L_1 are the input matching stage.

Inductor, L_5, and capacitor, C_3 is connected together to form inter-stage between first stage and second stage in order to improve flatness of the gain. Figure 3 illustrates the effect of L_7 on the gain flatness when the value of inductor is varied. It clearly can be seen that the flatness of ± 0.8 dB is achieved by choosing the values of L_7 to 147.5 pH.

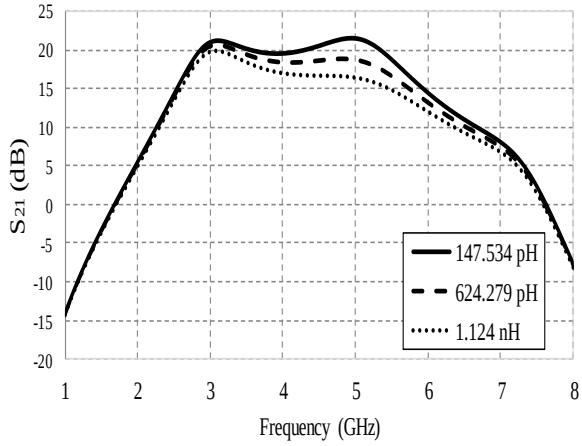

Figure 3: Effect of inductor L_7 towards gain

The technique used in second stage is a cascade common source that leads to very high gain at the desired signal frequency. Figure 4 shows the effect of cascaded common source towards gain. It can be seen from the simulation, the gain increase approximately twice the performance of current reuse technique that is used in first stage. Finally, the capacitor C_4 is used as dc block.

Table 2 shows the component parameters that are used in the proposed design including biasing, supply voltage, size of transistor, capacitor, resistor and inductor.

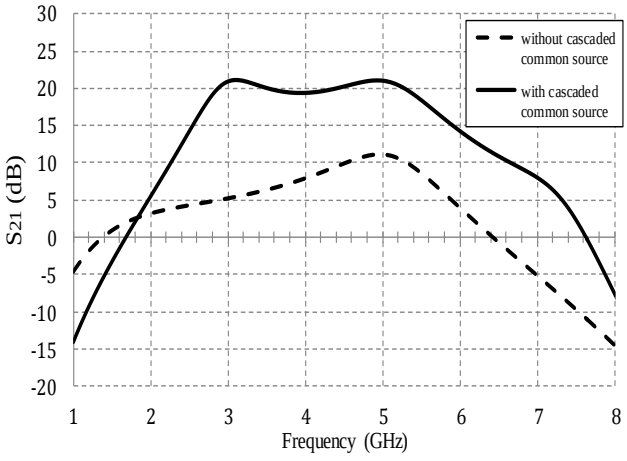

Figure 4: Effect of cascaded common source towards gain

Table 2
Component Parameters for Proposed PA

Component	Parameter
M_1, M_2	60 µm
M_3	120 µm
C_1	4.5 pF
C_2	2.8 pF
C_3	1.1 pF
C_4	2.0 pF
L_1	4.6 nH
L_2	147.5 pH
L_3	5.6 nH
L_4	7.1 nH
L_5	5.8 nH
L_6	1.9 nH
L_7	218.3 pH
V_{bias1}	1 V
V_{bias2}	1.8 V

III. RESULTS AND DISCUSSIONS

The proposed PA design was simulated in 0.13 µm CMOS technology with 1.8 V supply voltage. CADENCE SpectreRF simulator was used to simulate the proposed PA circuit.

Figure 5 is the simulation of S-parameters (i.e, S_{21}, S_{11} and S_{22}). It can be observed that the simulated gain of the proposed PA has very high gain of 20.3 dB with good flatness of ± 0.8 dB over frequency of 3.1 to 5.1 GHz. Input return loss, S_{11} and output return loss, S_{22} of less than -1.5 dB and less than -6 dB, respectively is achieved. In order to enhance the input return loss, the external input and output matching circuit can be employed in the proposed PA design. As depicted in Figure 6, good reverse isolation of -69.3 dB from 3.1 to 5.1 GHz is obtained. It shows that high reverse isolation, S_{12} can prevent LO leakage signal from transmitting to the antenna. It can be seen that group delay variation of ±121.3 ps is achieved as illustrated in Figure 7. This means that the output retain its original identity and suitable for UWB pulse radio system application. Figure 8 illustrates the stability factor of PA design. The PA design is unconditionally stable due to the value of K factor is larger than 1.

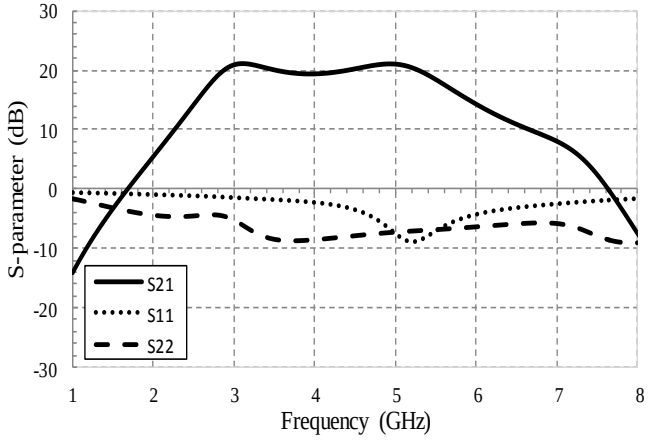

Figure 5: Measured S-parameters

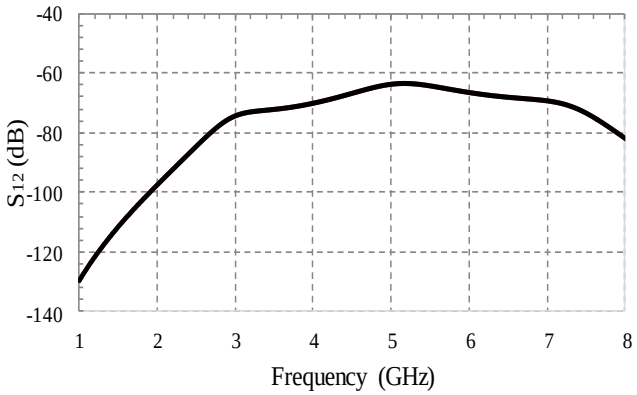

Figure 6: Measured reverse isolation

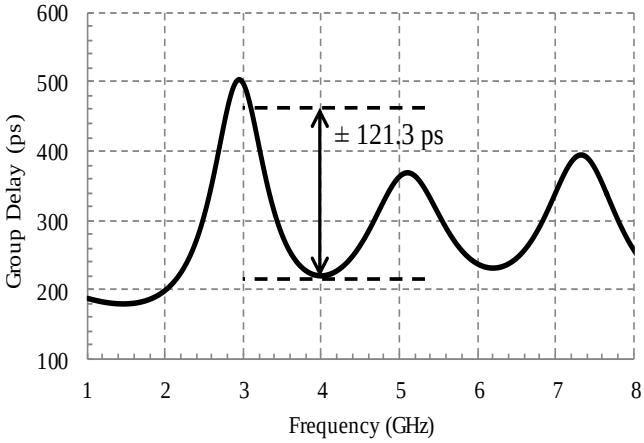

Figure 7: Measured group delay versus frequency

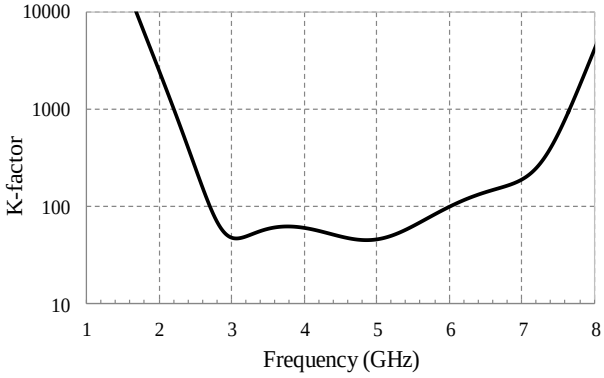

Figure 8: Measured stability versus frequency

The performance and comparison of previous reported UWB CMOS PAs with this proposed work is summarizes in Table 3. As can been seen that this proposed power amplifier has obtained a high gain with average gain flatness of 20.3 ± 0.8 dB, the power consumption of 27.3 mW as formulated in (2), good group delay of ± 121.3 ps compared to other researchers. This indicates that the proposed PA design is meet the DS-UWB specification.

Table 3
Performance summary and comparison of UWB CMOS PAs.

Ref. & Year	Techniques	Technology (µm)	V_{dd} (V)	Frequency (GHz)	Gain , S_{21}(dB)	S_{11} (dB)	S_{22} (dB)	Power consumption (mW)	Group delay (ps)
[16] 2009	Current reuse	0.18	1.0	3.1-4.8	18.4±1	<-5	<-5	22	N/A
[22] 2011	Resistive feedback and shun peaking	0.18	1.8	3.1-6.0	10±1	<-6.0	<-7	30	±195.5
[9] 2013	Resistive feedback	0.18	1.0	3.1-10.6	12.4±1.1	<-8.6	<-8.6	19	±18.3
[16] 2012	Stagger tuning & resistive shunt feedback	0.18	2.5	3.1-10.6	11.48±0.6	<-10	<-14	100	±85.8
[23] 2012	Shuntshunt feedback and shunt peaking	0.18	1.8	0.7-6.0	20	<-10	<-5	N/A	N/A
[17] 2015	Current reuse & stagger tuning	0.18	1.8	5.0-10.6	14±1	<-5.5	<-7	20	±40
This work	Current reuse	0.13	1.8	3.1-5.1	20.3±0.8	<-1.5	<-6	27.3	±121.3

IV. CONCLUSION

High gain of 3.1 GHz to 5.1 GHz UWB PA was designed and simulated by employing 0.13 µm CMOS technology. The current reused technique and cascaded common source configuration really helps in increasing the gain at the upper end of the desired band. Moreover, high gain achieved has good flatness, and low power consumption and good group delay for the desired frequency range.

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