

## EFFECT OF PROCESS PARAMETER VARIATION ON $f_t$ IN CONVENTIONAL AND JUNCTIONLESS GATE-ALL-AROUND DEVICES

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### Abstract

In this paper we have studied the effect of process variations on unity gain cut-off frequency ( $f_t$ ) in conventional and junctionless gate-all-around (GAA) transistors using TCAD simulations. Three different geometrical parameters, channel doping, source/drain doping (for conventional GAA), wire doping (for junctionless GAA) and gate electrode work function are studied for their sensitivity on  $f_t$ . For conventional GAA,  $f_t$  is more sensitive to gate length and source/drain doping and less sensitive to gate oxide thickness, ovality and channel doping and least sensitive to gate work function variations. For junctionless GAA,  $f_t$  is more sensitive to gate length and gate work function variations and less sensitive to gate oxide thickness, ovality, wire doping. The non-quasi static (NQS) delay is extracted for the most sensitive parameters. The trend of NQS delay is just the reverse trend of  $f_t$ .

Keywords: Gate-All-Around device, Junctionless GAA device, Non-Quasi Static delay, Unity gain cut-off frequency, TCAD.

### 1. Introduction

As downscaling of MOSFETs approaches the end of the ITRS, the silicon nanowire (SiNW) transistor with multi-gate or gate-all-around (GAA) architecture is attractive as one of the promising candidates for future CMOS technology. However as the device size is continuously scaled down, the formation of extremely abrupt junctions between source/drain and channel regions is still very challenging, even for the NW FETs when operating in the inversion-mode regime. But still, an ultrathin and narrow body (nanowire) MOSFET, when combined with the GAA structure, is deemed to be a major

**Nomenclatures**

$C_{gg}$	Gate Capacitance, fF
$f_i$	Unity gain cutoff frequency, GHz
$g_m$	Trans-conductance, mS
$I_{off}$	Off-state leakage current, A/ $\mu\text{m}$
$I_{on}$	On-state drive current, $\mu\text{A}/\mu\text{m}$
$L_g$	Gate length, nm
$N_{ch}$	Channel doping, / $\text{cm}^3$
$N_{SD}$	Source/Drain doping, / $\text{cm}^3$
$N_W$	Wire Doping, / $\text{cm}^3$
$T_{OX}$	Gate oxide thickness, nm
$V_{dd}$	Supply voltage, V
$V_{gs}$	Gate Source Voltage, V
$V_t$	Threshold voltage, V

**Abbreviations**

CMOS	Complementary Metal Oxide Semiconductor
GAA	Gate All Around
ITRS	International Technology Roadmap for Semiconductors
NQS	Non-quasi static
SDE	Sentaurus Structure Editor
SDEVICE	Sentaurus Device
SiNW	Silicon Nanowire
TCAD	Technology Computer Aided Design
WF	Work Function

candidate for extreme CMOS scaling provided the process complexities such as fabrication of short wires and the gate definition under the body are solved [1]. To go below 10 nm, GAA transistors are seen as the best option.

The structure that theoretically offers the best possible control of the channel region by the gate, and hence the best possible Electrostatic Integrity is the surrounding-gate MOSFET. The reduction in channel width and thickness can further increase the effectiveness of the gate control, i.e., the gates can effectively control the electrostatic potential in the ultrathin channel, so that the channel suffers from lesser electrical interference between source and drain [2, 3]. Due to this, GAA device has enhanced drive current and sub threshold slope, as well as good immunity to short-channel effects.

There are some experimental results in the literature showing lithographically defined fully CMOS compatible silicon nanowire GAA device n- and p-MOS transistors with nanowire channel in different crystal orientations and characterized at various temperatures down to 5 K. These nanowire devices show high drive current, and excellent gate control with high  $I_{on}/I_{off}$  ratio. PMOS GAA device shows  $I_{on}$  enhancement along  $\langle 010 \rangle$  orientation in comparison to conventional  $\langle 110 \rangle$  direction [4]. The work function of the metal gate material used for GAA device is from 4.2 eV to 5.5 eV [5].

Literature is available for GAA, which can be particularly used for reducing the problems of conventional multi-gate FinFET, improving device performance

and scaling down capabilities [6, 7]. Surrounding-gate SOI MOSFETs with a gate length as small as 5 nm and a diameter of 3 nm have shown to be fully functional [8]. RF performance of GAA device has been investigated by [9]. Junctionless GAA devices have been explored recently [10, 11]. A systematic sensitivity analysis of conventional and junctionless GAA device RF performance is yet to be investigated. For RF applications unity gain cut-off frequency ( $f_i$ ) is one of the important metric and it is the frequency at which  $|Y_{21}/Y_{11}|$  ratio equals one. In terms of device parameters,  $f_i$  is given by  $g_m/C_{gg}$  where  $g_m$  is transconductance,  $C_{gg}$  is the combination of gate-source capacitance ( $C_{gs}$ ), gate-drain capacitance ( $C_{gd}$ ) and overlap capacitance ( $C_{ov}$ ) [12].

In this paper, the effect of various process parameters on  $f_i$  is studied systematically. Three different geometrical parameters and three non-geometrical parameters (related to conventional GAA device) and two non-geometrical parameters (related to junctionless GAA device) are varied to capture their sensitivity on  $f_i$ . The non-quasi static (NQS) delay is extracted for the most sensitive parameters. The outline of this paper is as follows. Next section deals with the description and calibration of the devices. Section 3 explains about the parameter space for sensitivity study. Section 4 discusses the simulation results. Finally in Section 5 the conclusions are provided.

## 2. Device Description and Calibration

Sentaurus TCAD simulator from Synopsys [13] is used to perform all the simulations. All the simulations are carried out at 3D level. The device structures are generated using Sentaurus Structure Editor (SDE). Figure 1(a) shows the 3-D structure of the GAA device. The front view is shown in Fig. 1(b). The cross sectional views along the channel are given in Figs. 1(c) and (d), for conventional and junctionless GAA devices respectively. From Fig. 1(c) it can be seen that the channel is of p type doping and it has a doping concentration of  $1 \times 10^{16}/\text{cm}^3$  whereas source/drain are n<sup>+</sup> doping and the doping concentration ranges to  $1 \times 10^{20}/\text{cm}^3$ . For Fig. 1(d), there is a uniform doping (n<sup>+</sup>) of  $6 \times 10^{19}/\text{cm}^3$  throughout the entire device.

Device simulator (SDEVICE) includes the appropriate models for band to band tunnelling, quantization of inversion layer charge, doping dependency of mobility, effect of high and normal electric fields on mobility, and velocity saturation. Standard AC simulations are done in SDEVICE and  $f_i$  is extracted from these results. As already stated,  $f_i$  is the frequency at which  $|Y_{21}/Y_{11}|$  equals one, and it strongly depends on the gate bias. At various gate biases  $f_i$  is calculated and the maximum of them is taken as  $f_i$ . The current values of the two devices are calibrated against the ITRS [14]. The device dimensions are given in Table 1. From Table 1 it can be seen that the two devices differ with respect to their doping concentrations and work functions. Conventional GAA device has two different doping concentrations for channel ( $1 \times 10^{16}/\text{cm}^3$ ) and source/drain ( $1 \times 10^{20}/\text{cm}^3$ ) whereas junctionless GAA device has a uniform heavily doped concentration ( $6 \times 10^{19}/\text{cm}^3$ ).

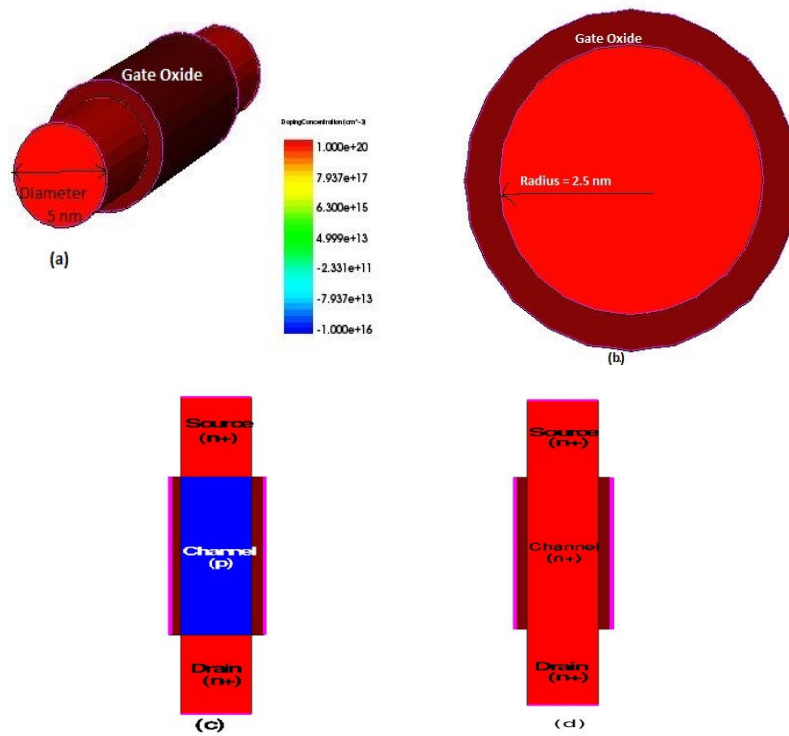


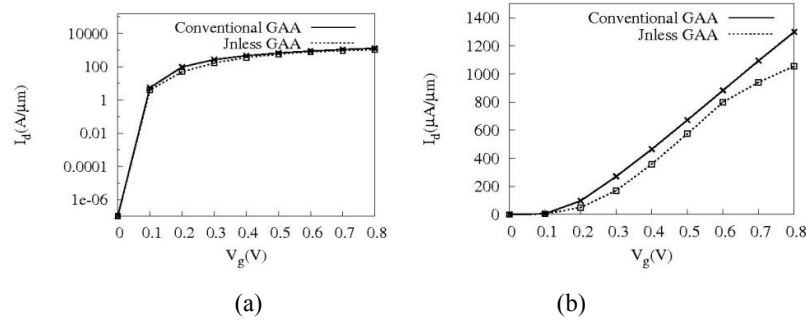
Fig. 1. (a) 3-D structure of GAA device (b) The front view of GAA device (c) Cross-sectional view along the channel of conventional GAA device (d) Cross-sectional view along the channel of junctionless GAA device.

Table 1. Dimensions of conventional and junctionless GAA.

Process Parameters	Conventional GAA device	Junctionless GAA device
Gate Length ( $L_g$ )		17 nm
Diameter ( $D$ )		5 nm
Gate oxide thickness ( $T_{ox}$ )		0.77 nm
Ovality	1 (ratio between major and minor axes)	
Channel doping ( $N_{ch}$ )	$1 \times 10^{16}/\text{cm}^3$	
Source/Drain doping ( $N_{SD}$ )	$1 \times 10^{20}/\text{cm}^3$	$6 \times 10^{19}/\text{cm}^3$
Gate Work Function ( $WF$ )	4.27 eV	4.63 eV
Supply Voltage ( $V_{dd}$ )		0.8 V

Figure 2(a) shows the simulated  $I_d-V_g$  characteristics for conventional and junctionless GAA devices in log scale. Both the devices are matched to have same leakage current ( $I_{off}$ ) of 100 nA/ $\mu\text{m}$ . Figure 2(b) shows the  $I_d-V_g$  characteristics in linear scale. It can be observed that the junctionless GAA devices have less drive current (1300  $\mu\text{A}/\mu\text{m}$  for conventional GAA and 1056

$\mu\text{A}/\mu\text{m}$  for junctionless GAA) compared to the conventional GAA devices for the same  $I_{off}$ . The mobility of junctionless devices is lower compared to inversion mode devices [15] and leads to higher drive current ( $I_{on}$ ) in inversion mode devices. Since the carrier transport is in the bulk of the semiconductor, the current is reduced in the junctionless device. This in turn reduces the impact of imperfect semiconductor/insulator interfaces [16]. The extremely low leakage current is responsible for the susceptibility of short channel effects in junctionless devices.



**Fig. 2. (a) Simulated  $I_d$ - $V_g$  characteristics of GAA devices of gate length 17 nm with  $I_{off} = 100 \text{ nA}/\mu\text{m}$  (log scale) (b) Simulated  $I_d$ - $V_g$  characteristics of GAA devices of gate length 17 nm (linear scale).**

### 3. Parameter Space for Sensitivity Study

The process parameters considered here are gate length ( $L_g$ ), gate oxide thickness ( $T_{ox}$ ), ovality, channel doping ( $N_{ch}$ ), source/drain doping ( $N_{SD}$ ) and gate work function (WF). Ovality (non-circularity) is the degree of deviation from perfect circularity of the cross-section of the cylinder. These six parameters are varied over a range of values to capture their sensitivity on  $f_i$  for conventional and junctionless GAA devices. For junctionless devices, source/drain doping and channel doping are not considered separately and can be combined together called wire doping ( $N_W$ ). Table 2 gives the range of values for the conventional and junctionless GAA devices.

**Table 2. Range of values for the conventional and junctionless GAA devices.**

Process Parameters	Conventional GAA device	Junctionless GAA device
Gate Length ( $L_g$ )	10 nm - 30 nm	
Gate oxide thickness ( $T_{ox}$ )	0.5 nm - 2 nm	
Channel doping ( $N_{ch}$ )	$1 \times 10^{15}/\text{cm}^3$ - $1 \times 10^{19}/\text{cm}^3$	
Source/Drain doping ( $N_{SD}$ )	$1 \times 10^{18}/\text{cm}^3$ - $2 \times 10^{20}/\text{cm}^3$	$3 \times 10^{19}/\text{cm}^3$ - $8 \times 10^{19}/\text{cm}^3$
Gate Work Function (WF)	4.1 eV - 4.7 eV	4.6 eV - 5.1 eV

From Table 2 it can be seen that the doping concentration and work functions are varying for both the devices with their lower and upper bounds. For conventional GAA devices, channel doping concentration varies from  $1 \times 10^{15}/\text{cm}^3$  to  $1 \times 10^{19}/\text{cm}^3$  and source/drain doping concentration varies from  $1 \times 10^{18}/\text{cm}^3$  to  $2 \times 10^{20}/\text{cm}^3$ . Since the doping concentration is uniform for junctionless GAA devices, it takes the value from  $3 \times 10^{19}/\text{cm}^3$  to  $8 \times 10^{19}/\text{cm}^3$ .

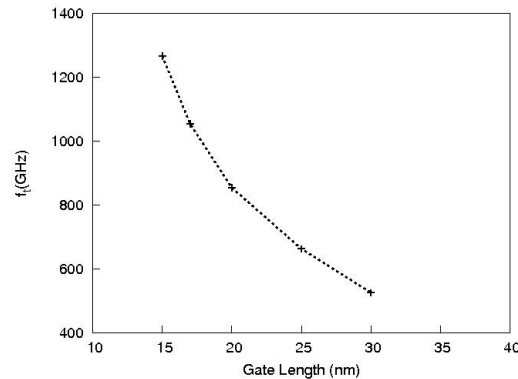
## 4. Results and Discussion

### 4.1. Sensitivity Analysis with respect to $f_i$ for conventional GAA device

As already stated, the six different process parameters are varied one at a time, and their sensitivity to  $f_i$  is analysed in this section.

#### Variation in gate length

Figure 3 shows the variation of  $f_i$  against gate length ( $L_g$ ). Conventional GAA devices have a monotonic decrease with respect to  $L_g$ . This is the expected behaviour. This can be reasoned out with the  $g_m$  degradation for higher gate lengths.



**Fig. 3. Variation of  $f_i$  with respect to gate length in conventional GAA device.**

#### Variation in gate oxide thickness

Figure 4 depicts the increase in  $f_i$  with respect to  $T_{ox}$ . Due to vertical gate electrical field, mobility degradation comes into picture with gate oxide scaling which ultimately decreases  $g_m$  although there is increase in  $C_{gg}$  [17]. Thus  $f_i$  decreases with gate oxide scaling.

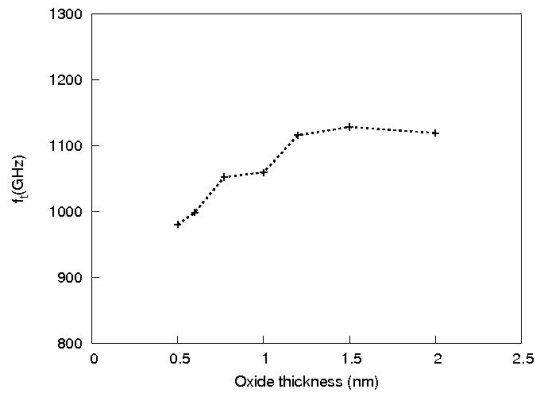
#### Variation in ovality

Figure 5 depicts the variation of  $f_i$  with respect to ovality. It can be seen from Fig. 5 that there is a slight increase in  $f_i$  with respect to ovality. The variation in the ovality affects the channel width which in turn affects  $g_m$ . The increase in  $g_m$  increases  $f_i$ .

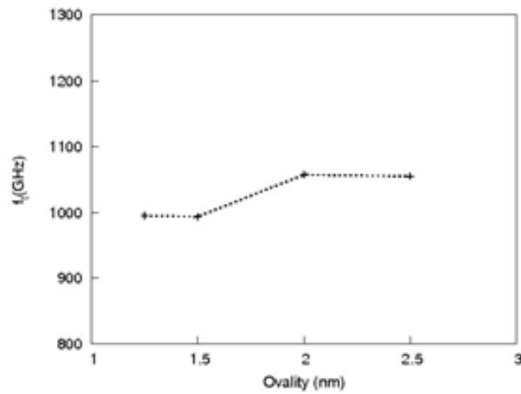
#### Variation in channel doping

Figure 6 shows the variation of  $f_i$  against  $N_{ch}$ .  $f_i$  is least sensitive at lower channel doping levels, similar to that of double gate FinFET, which is studied in [18]. At

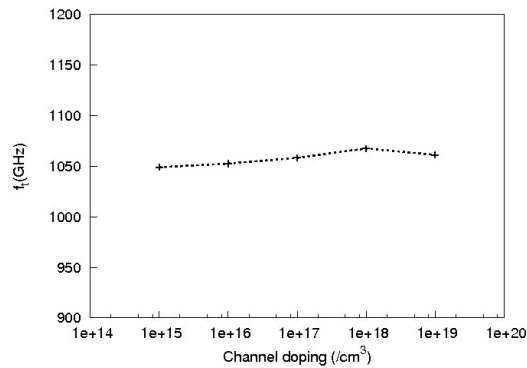
higher doping levels,  $f_i$  is slightly decreasing due to  $g_m$  degradation. The same is seen in Fig. 6.



**Fig. 4. Variation of  $f_i$  against gate oxide thickness in conventional GAA device.**



**Fig. 5. Variation of  $f_i$  with respect to ovality in conventional GAA device.**



**Fig. 6.  $f_i$  versus channel doping in conventional GAA device.**

### Variation in source/drain doping.

When  $N_{SD}$  increases,  $I_{on}$  and  $g_m$  increase due to the lowered parasitic series resistance and thereby  $f_t$  is expected to increase. Figure 7, which shows the variation of  $f_t$  with  $N_{SD}$ , reflects the same.

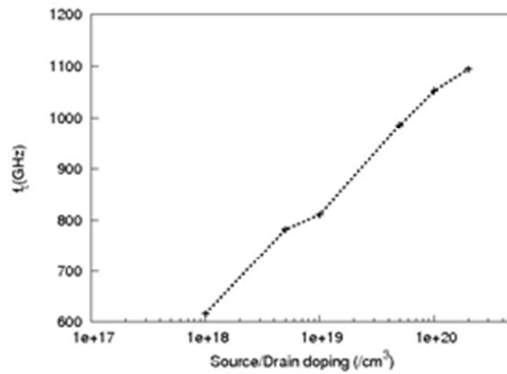


Fig. 7.  $f_t$  versus Source/drain doping in conventional GAA device.

### Variation in gate work function

Screening effect is observed in the conventional GAA devices, similar to that of FinFET, which is explored by Lakshmi and Srinivasan [19]. Therefore,  $f_t$  is expected to be constant or least sensitive to gate electrode work function. The same can be observed in Fig. 8 which depicts the graph between  $f_t$  and work function.

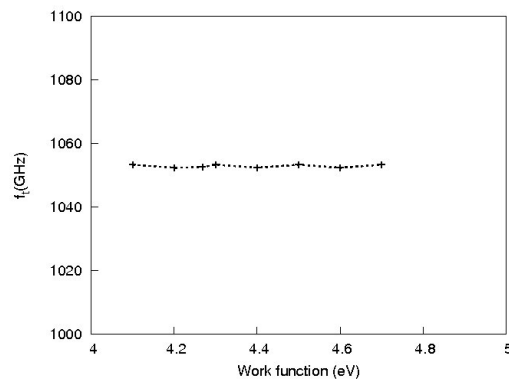


Fig. 8. Variation of  $f_t$  with gate electrode work function in conventional GAA device.

## 4.2. Sensitivity Analysis with respect to $f_t$ for junctionless GAA device

The five parameters of junctionless GAA device are varied as shown in Table 2 and their sensitivity to  $f_t$  is analysed in this section.



### Variation in gate length

Figure 9 shows the variation of  $f_i$  against gate length ( $L_g$ ). Junctionless GAA devices have a monotonic decrease with respect to  $L_g$ . This can be reasoned out with the  $g_m$  degradation for higher gate lengths which is an expected result. From Fig. 9 it can be seen that the junctionless devices show lesser  $f_i$  ( $f_i = 620$  GHz for  $L_g = 20$  nm) compared to the conventional devices ( $f_i = 850$  GHz for  $L_g = 20$  nm) and this has been reported by Lakshmi and Srinivasan [20].

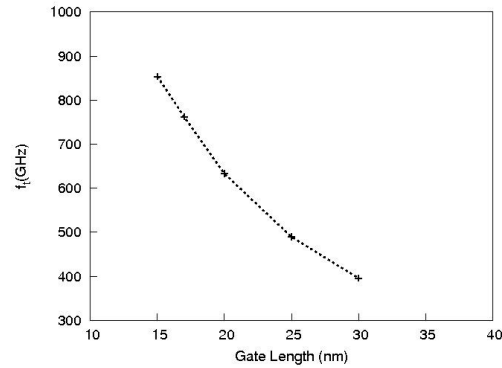


Fig. 9. Variation of  $f_i$  with respect to gate length in junctionless GAA device.

### Variation in gate oxide thickness

Figure 10 shows the variation of  $f_i$  with gate oxide thickness ( $T_{ox}$ ). The mobility degradation is less in the junctionless devices [21]. Therefore this device does not show any significant decrease for thin oxides.

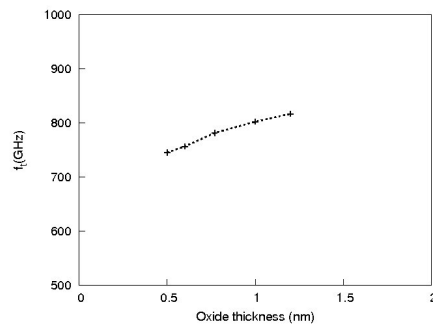


Fig. 10. Variation of  $f_i$  against gate oxide thickness in junctionless GAA device.

### Variation in Ovality

Figure 11 depicts the variation of  $f_i$  with respect to ovality. Similar to the conventional GAA device, the variation in the ovality affects the channel width which in turn affects  $g_m$  thereby increases  $f_i$  slightly.

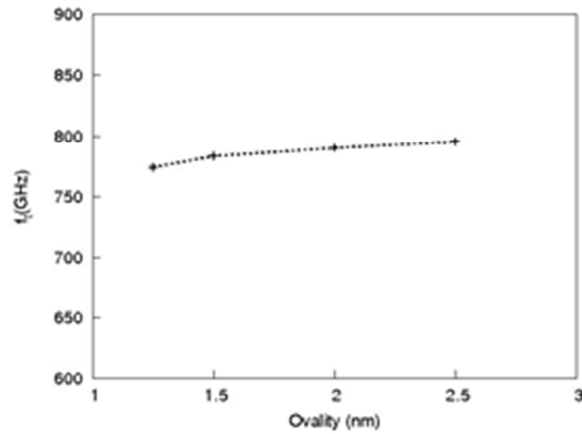


Fig. 11. Variation of  $f_i$  against ovality in junctionless GAA device.

### Variation in Wire Doping

Figure 12 shows the variation of  $f_i$  against wire doping. For the junctionless devices, we can make the sensitivity study only for a limited range ( $3 \times 10^{19}/\text{cm}^3$  -  $8 \times 10^{19}/\text{cm}^3$ ). Beyond this range,  $f_i$  occurs at the extreme gate voltages, i.e., either at very low gate voltage or at  $V_{dd}$ . In this range,  $f_i$  is less sensitive to wire doping.

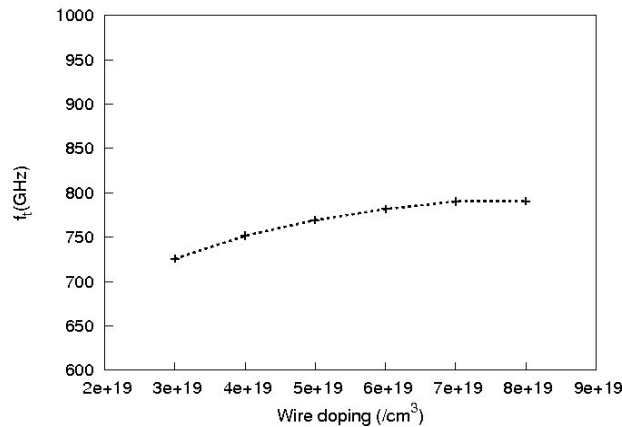
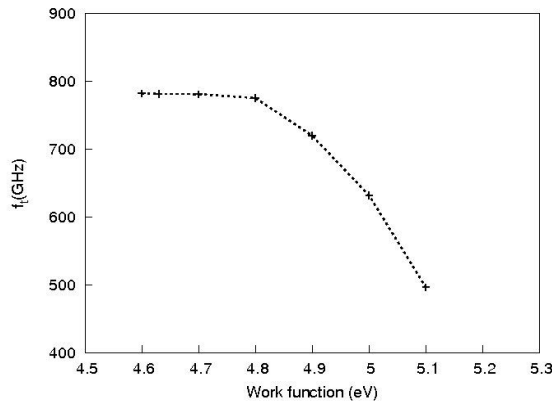


Fig. 12.  $f_i$  versus wire doping in junctionless GAA device.

### Variation in gate work function

Figure 13 plots the variation of  $f_i$  with respect to gate work function. It can be observed that  $f_i$  starts to decrease after certain work function range. Junctionless devices have a strong dependency of  $f_i$  with respect to work function because there is no screening effect from the inversion region. Table 3 shows the classification of the various process parameters based on their sensitivity.



**Fig. 13. Variation of  $f_t$  with gate electrode work function in junctionless GAA device.**

**Table 3. Classification of the Process Parameters based on their Sensitivity to  $f_t$  in Conventional and Junctionless GAA devices.**

Conventional GAA device			Junctionless GAA device	
Gate Length	Oxide thickness	Gate Work function	Gate Length	Oxide thickness
Source/Drain Doping	Ovality		Gate Work function	Ovality
	Channel Doping			Wire doping

**4.3. NQS delay for the sensitive parameters**

For the sensitive parameters given in the Table. 3, NQS delay is extracted at a frequency of 200 GHz. To reason out the simulation result, the expression given by Allen et al [22] is used. For a particular NQS delay, the NQS frequency ( $f_{NQS}$ ) is given by

$$f_{NQS} = \frac{\alpha \mu_{eff} (V_{GS} - V_t)}{2\pi L_g^2} \tag{1}$$

where  $\alpha$  is the fitting parameter,  $\mu_{eff}$  the mobility,  $V_{GS}$  the gate bias and  $V_t$  the threshold voltage of the transistor.

**Conventional GAA device**

The most sensitive parameters in conventional GAA device are found out to be  $L_g$  and  $N_{SD}$ . For these parameters alone, the NQS delay is extracted at a frequency of 200 GHz. Figure 14 shows the variation of NQS delay with respect to gate length. It can be seen that the delay increases with respect to  $L_g$ . Equation 1 predicts that

as  $L_g$  increases  $f_{NQS}$  decreases, i.e., for the given frequency NQS delay increases. Figure 15 shows the variation of NQS delay with respect to source/drain doping. The delay decreases for the variation in source/drain doping, which can be reasoned out similar to Fig. 7.

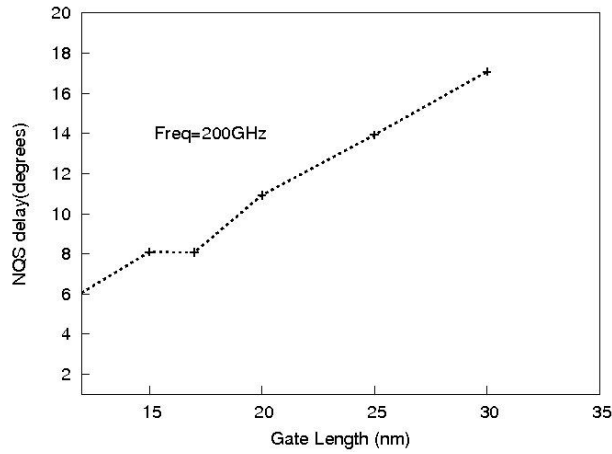


Fig. 14. NQS delay vs gate length in conventional GAA device.

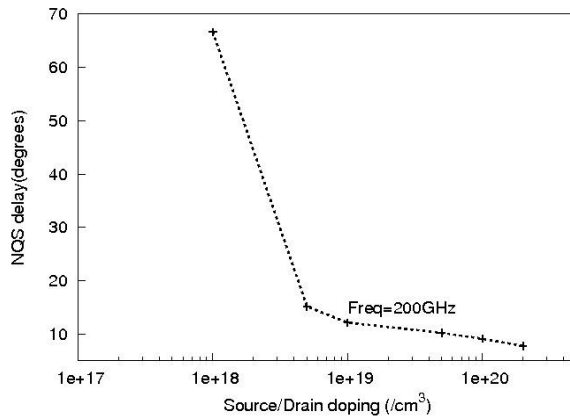


Fig. 15. NQS delay vs source/drain doping in conventional GAA device.

**Junctionless GAA device**

The most sensitive parameters in junctionless GAA device are found out to be  $L_g$  and WF. Figure 16 shows the variation of NQS delay with respect to gate length. As discussed previously, the delay increases monotonically with respect to gate length for junctionless GAA device also. Figure 17 shows the variation of NQS delay with respect to gate electrode work function. The increase in the

work function increases  $V_t$ , which ultimately increases the delay except for some initial values.

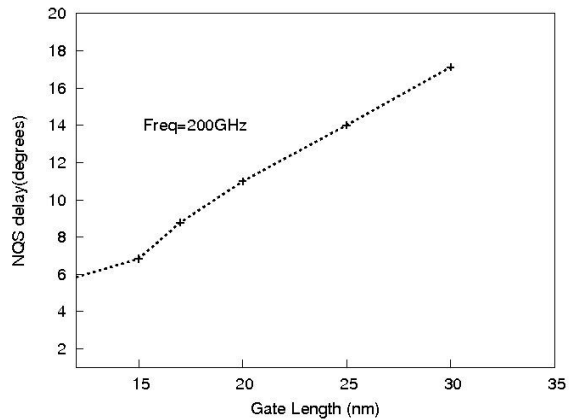


Fig. 16. NQS delay vs gate length in junctionless device.

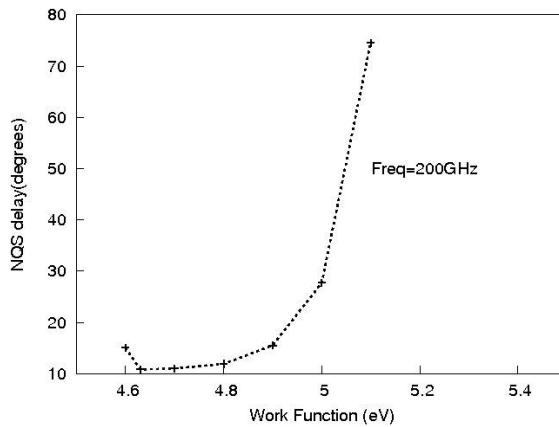


Fig. 17. NQS delay vs work function in junctionless GAA device.

## 5. Conclusion

In this paper, three different geometrical parameters and three non-geometrical parameters have been varied over a range and their effects on  $f_t$  have been studied for conventional and junctionless GAA. It was found that for conventional GAA,  $f_t$  is more sensitive to gate length and source/drain doping and less sensitive to gate oxide thickness, ovality and channel doping and least sensitive to gate work function variations. For junctionless GAA,  $f_t$  is more sensitive to gate length and gate work function variations and less sensitive to gate oxide thickness, ovality, wire doping. For the most sensitive parameters, NQS delay is extracted and the

trend followed by the NQS delay is just the reverse of  $f_t$ .

### Acknowledgement

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