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Optimisation of Process Parameters for Lower Leakage Current in 22 nm n-type MOSFET Device using Taguchi Method

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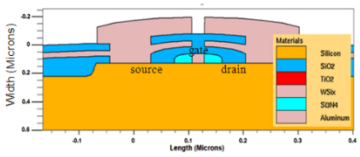
Graphical abstract



Abstract

In this article, Taguchi orthogonal array method was used to optimize the process parameters during the design of a 22 nm n-type Metal Oxide Semiconductor Field Effect Transistor (MOSFET) in order to decrease the leakage current (I_{LEAK}) of the device. Titanium dioxide (TiO_2) was used as the dielectric layer to replace the traditional silicon dioxide SiO_2 and tungsten silicide (WSi_x) was used as a metal gate to replace polysilicon. The device's fabrication and electrical characterization were executed using ATHENA and ATLAS modules from Silvaco International. Taguchi's Power of Three Series L9 orthogonal array was used to optimize the device process parameters and to finally predict the best process parameter combination to obtain the minimum leakage current (I_{LEAK}) using Smaller-the-Better (STB) signal-to-noise ratio (SNR). The optimization resulted in the attainment of the lowest I_{LEAK} mean value of 0.25759 nA/µm which is in accordance to the predicted value given in the International Technology Roadmap for Semiconductors (ITRS) 2011.

Keywords: Taguchi Method; 22 nm n-type MOSFETs; high-k/metal gate; leakage current; Silvaco software

Abstrak

Dalam artikel ini, kaedah tatasusunan Taguchi orthogonal telah digunakan untuk mengoptimumkan parameter proses semasa mereka bentuk 22 nm jenis-n Transistor Kesan Medan Semikonduktor Oksida Logam (MOSFET) untuk mengurangkan arus pembocoran perkakas. Titanium diokside ((TiO_2)) telah digunakan sebagai lapisan diaelektrik untuk menggantikan silikon dioksida tradisional SiO_2 dan tungsten silicide (WSi_x) telah digunakan sebagai get logam untuk menggantikan polisilikon. Fabrikasi perkakasan dan pencirian elektrikal telah dijalankan menggunakan modul ATHENA dan ATLAS dari Silvaco Antarabangsa. Kuasa Taguchi daripada tatasunan orthogonal tiga siri L9 telah digunakan untuk mengoptimumkan parameter proses perkakas dan akhirnya menjangkakan parameter proses yang terbaik untuk mencapai minimum arus pembocoran (I_{LEAK}) menggunakan Lagi Kecil-Lagi Bagus (STB) nisbah Isyarat-kepada-bising (SNR). Pengoptimuman telah menghasilkan pencapaian 0.25759 nA/µm iaitu menurut nilai jangkaan dalam Pelan Hala Tuju Teknologi Semikonduktor Antarabangsa (ITRS) 2011.

Kata kunci: Kaedah Taguchi; 22 nm jenis-n MOSFETs; get thinggi-k/logam; arus pembocoran; perisian Silvaco

1.0 INTRODUCTION

Since the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is the most important device in many circuits such as microprocessors, memory circuit and so on, the research and development to improve the performance of this device is growing at an unprecedented rate. One crucial method to improve its performance is to design it in small dimensions, which means to downscale the device. At the same time smaller devices can be implemented in a smaller area of integrated circuits (ICs) and this leads to increasing the number of transistor-per-wafer. But the downsizing of the transistor's dimensions' also requires the reduction of the gate dielectric thicknesses.

The silicon dioxide (SiO_2) layer has been used as a gate dielectric material over decades. The reduction of the equivalent oxide thicknesses (EOT) until 1nm makes it impossible for SiO_2 to be fabricated since this thickness causes higher gate leakage current to occur and subsequently increasing the current densities and encourages high power dissipation [1]. The phenomenon of device downscaling has resulted in the drain area to be much closer to the source thereby introducing short channel effects which leads to increase in the leakage current [2]. Gate leakage

current problems can be solved by the introduction of a combination of high permittivity (high-k) gate dielectric and metal gate [3].

Therefore, replacement of the SiO_2 and polysilicon layers with high-k and metal gate materials respectively solves one of the major challenges for further downscaling in order to keep planar MOSFET devices still on track [4]. There are a number of high-k materials being proposed and analyzed as the replacement of SiO_2 in the next generation of MOSFETs. In this experiment, TiO_2 and WSi_x were utilized as the high-k dielectric material and the metal gate respectively. As a benchmark for device performance, the device characteristic prediction made by the ITRS gives a good reference to researchers to continue discovering and developing the MOSFET technology.

In our previous work, we successfully optimized the threshold voltage (V_{th}) in designing a 22 nm NMOS transistor using the L_9 Taguchi method of Nominal-the-Best (NTB) signal-to-noise ratio SNR [5]. With this motivation, we continue our optimization process in an effort to reduce I_{LEAK} using Taguchi method. In the pursuit of downscaling CMOS devices with low threshold voltages, the I_{LEAK} has been identified as one of the dominant sources of leakage to the total power consumption of CMOS devices [6]. One reported that leakage current can be as low as 1.858 nA/µm for 22 nm n-type MOSFET device [7]. Taguchi method is well suited to solve multiple control factor optimization problems with less number of experiments. This method uses a special design of orthogonal arrays in order to study the multiple process parameters with less number of experiments [8, 9]. With added noise factors called signal-to-noise ratio (SNR), device optimization using Taguchi method becomes more reliable.

There are three types of SNR performance characteristics, that is Nominal-the-Best, Larger-the-Better and Smaller-the-Better [10]. Based on the SNR performance characteristics, the larger the SNR results the better the performance characteristic. This means that, the level of each process parameter which has the highest SNR shows the optimum level of the design. Moreover, an analysis of variance (ANOVA) is executed in order to identify the most significant value of the process parameter. With the combination of the SNR and ANOVA analysis, the best combination of process parameter in designing the device can be predicted finally. As the target in this paper is to optimize and obtain minimum I_{LEAK}, SNR of Smaller-the-Better (STB) analysis was utilized.

In this experiment, an L9 orthogonal array that consists of four process parameters which are the Halo implantation, Source/Drain (S/D) implantation, the compensation implantation and the threshold voltage (V_{th}) adjust implantation were used. The Sacrificial Oxide Layer (PSG) temperature and the P-well implantation temperature were identified as the noise factors in order to get the optimized process parameters. The aim of the current work is to minimize the I_{LEAK} of the device in order to meet the ITRS 2011 prediction for 22 nm n-type MOSFET where the accepted maximum value for I_{LEAK} is 100 nA/µm [11].

■2.0 MATERIALS AND METHODS

2.1 Fabrication Simulation

The fabrication process steps are as follows. A p-type silicon substrate with <100> orientation is used and a P-well region using Boron as a dopant with a dose of 3.75×10^{12} ions/cm^2 is produced. Then a 130 Å thickness of the Shallow Trench Isolator (STI) was produced by oxidizing the wafer in dry oxygen for 25 minutes followed by a low pressure chemical vapour deposition process (LPCVD) and etching process [12]. The next step was to implant the N-well active area, with boron dose of 6.98×10^{12} ions/cm^2, followed by halo implantation process by indium dose of 12.75×10^{12} ions/cm^2. The dosage was varied in order to get the optimum value [13]. Then the high-k material, TiO_2 (dielectric permittivity, ε_{opt} = 5.4) was deposited for a final thickness of 2 nm [14] and this is followed by etching to get the desired thickness and was adjusted to produce a 22 nm gate length. WSi_x was utilized as the metal gate was then deposited on the top of the bulk device. Then, side wall spacers were formed where it functions as a mask for the source and drain implantation [15]. Then, there are source-drain implantations where Arsenic was firstly implanted with a dose of 5.15×10^{13} ions/cm^2, followed by phosphorous with a dosage of 1.75×10^{12} ions/cm^2. The next process was the development of 0.5 µm Borophosphosilicate Glass (BPSG) layer that acts as a pre-metal dielectric (PMD) [16]. After BPSG deposition, the wafer undergoes annealing process at a temperature of 850°C [17]. The next process was compensation implantation using phosphorous, with a dosage of $3.65x10^{13}$ ions/cm^2 [17]. Then lastly, aluminium layer was deposited on top of the structure. Then, the transistor undergoes electrical characteristic process using ATLAS simulation module in order to study the leakage current of the device with reference to ITRS 2011 [11].

2.2 Taguchi L9 Orthogonal Array Method

Taguchi method is used to optimize the process parameters to achieve the best combination of the process parameter in order to attain the perfect device performance with less number of experiments. In this study, the Taguchi Method L9 orthogonal arrays are applied to explore the process parameters in designing 22 nm n-type MOSFET with the target to achieve minimum leakage current, I_{LEAK}.

2.3 Ideal Function and P-Diagram

In this case, the dynamic ideal function is used where the dynamic ideal function equation is given by, $y = \beta M$ [18], where y is the output response where in this case is the I_{LEAK} value. M is the input signal which refers to the drain voltage that is internally applied in the simulation process. Beta, β is the measurement sensitivity to different inputs. The P-diagram is a block diagram that represents a process of product in order to achieve a robust design. Based on the P-diagram in Figure 1, the output response (y), is to achieve minimum I_{LEAK} by optimizing the control factors, C; and added with noise factors, N in order to make the process parameters insensitive to the design.

Since a minimum I_{LEAK} value is needed, the Taguchi L9 (3^4) orthogonal array consisting of 4 process parameters at 3 different levels with two noise factors were used. Therefore, a total of 36 runs are needed to optimize the device design. All the values of the process parameters and noise factors are listed in Table 1 and Table 2 respectively.

■3.0 RESULTS AND DISCUSSION

3.1 Fabrication Simulation Result

Based on the fabrication step in section 2.1, the result of the device simulation where the complete device for 22 nm n-type MOSFET and the device doping profile are shown on Figure 2 and Figure 3 respectively.

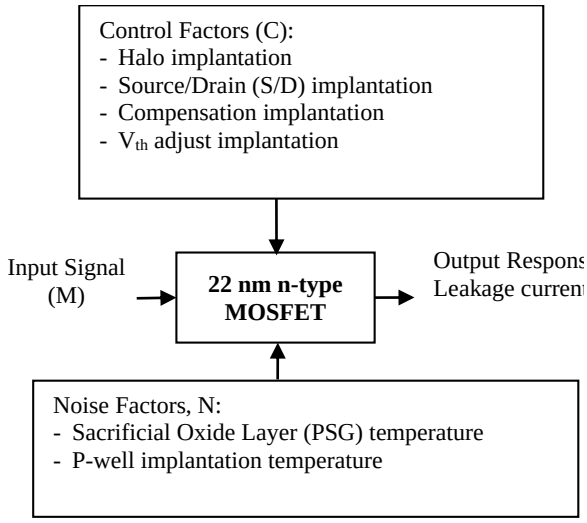


Figure 1 P-diagram of 22nm n-type MOSFET

Table 1 Process parameters and their levels

Symbol	Process Parameter	Level 1	Level 2	Level 3
		(atom/cm^3)		
A	Halo Implantation	1.270e^{13} (A1)	1.275 e^{13} (A2)	1.280 e^{13} (A3)
B	S/D Implantation	5.100e^{13} (B1)	5.150 e^{13} (B2)	5.200 e^{13} (B3)
C	Compensation Implantation	3.650 e^{13} (C1)	3.700 e^{13} (C2)	3.750 e^{13} (C3)
D	V_{th} Adjust Implantation	6.940 e^{12} (D1)	6.960 e^{12} (D2)	6.980 e^{12} (D3)

Table 2 Noise factors and their levels

Symbol	Noise Factor	Level 1	Level 2
		°C	
X	Sacrificial Oxide Layer	900 (X1)	902 (X2)
Y	P-well Implantation Temperature	850 (Y1)	852 (Y2)

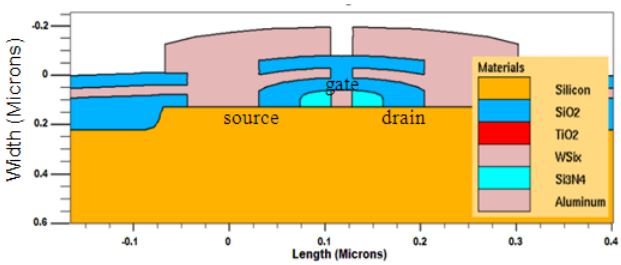


Figure 2 Completed figure of the 22 nm of n-type MOSFET

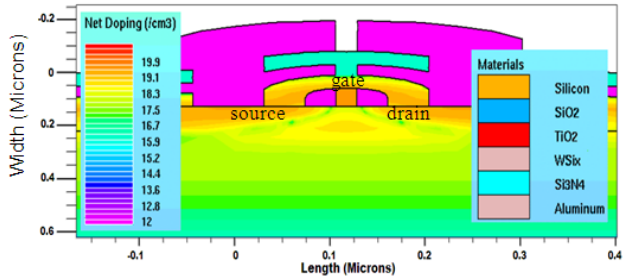


Figure 3 The doping profile of the 22 nm n-type MOSFET

3.2 Signal-to-Noise Ratio Analysis for 22nm n-type MOSFET Device

The L9 orthogonal array analysis for output response, I_{LEAK} was simulated and listed in Table 3. Once the result is obtained, the next step in Taguchi method is to analyze the output response using signal-to-noise ratio (SNR) of Smaller-the-Better [10]. The SNR (Smaller-the-Better), η_{STB} can be expressed as

$$\eta_{STB} = -10\log_{10}\left(\frac{1}{n}\sum_{i=1}^{n} y_i^2\right) \quad (1)$$

where n is number of tests and y_i is the experimental value of the leakage current. By applying the formula given in Equation (1) the η_{STB} for the device was calculated and given as in Table 4. The parametric combination level of the process and noise factors is also listed in Table 4.

Table 3 Output response, I_{LEAK} values for n-type MOSFET

Exp. No	Leakage current (nA/μm)			
	X1Y1	X1Y2	X2Y1	X2Y2
1	0.53388	0.55181	0.53465	0.55261
2	0.91165	0.94263	0.91297	0.94399
3	1.55757	1.61120	1.55983	1.61353
4	0.62211	0.64328	0.62298	0.64421
5	1.22233	1.26440	1.22410	1.26623
6	0.73231	0.75758	0.73336	0.75867
7	0.53134	0.55009	0.53209	0.55087
8	0.31947	0.33080	0.31993	0.33127
9	0.62467	0.64698	0.62556	0.64790

From the SNR analysis, we can evaluate the performance of the device characteristics. Generally, in SNR analysis, the highest value of the SNR in the experiment indicates that the experiment shows the best performance of the device. For that reason, the optimal level of the process parameters is the level with the highest SNR [10].

Table 4 SNR for I_{LEAK} and their main effects

Exp No.	SNR (dB)	Process Parameter Level			
		Halo Implant (A)	S/D Implant (B)	Compensation Implant (C)	V_{th} Adjust Implant (D)
1	185.30	1	1	1	1
2	180.65	1	2	2	2
3	176.00	1	3	3	3
4	183.97	2	1	2	3
5	178.10	2	2	3	1
6	182.55	2	3	1	2
7	185.33	3	1	3	2
8	189.75	3	2	1	3
9	183.93	3	3	2	1

By referring to Table 4, row 8 has the highest SNR value of 189.75 dB. The high value of SNR indicates that the process parameters in row 8 gives the best insensitivity for the response characteristics. Since the experimental design is orthogonal, the effect of each process parameter on the SNR at different levels can be separated out.

The SNR (Smaller-the-Better) response for each level in this experiment with total mean of the SNR is summarized in Table 5.

Table 5 SNR response for the I_{LEAK}

	Process Parameter	SNR (Smaller-the-Better)			Total Mean SNR
		Level 1	Level 2	Level 3	
A	Halo Implantation	180.65	181.54	186.34	182.84
B	S/D Implantation	184.87	182.83	180.82	
C	Compensation Implantation	185.87	182.85	179.81	
D	V_{th} Adjust Implantation	182.44	182.84	183.24	

From the data in Table 5, the factor effect graph for the SNR (Smaller-the-Better) of the experiment is plotted in Figure 4. The dashed horizontal lines in the graph represent the values of the total mean of the SNR (Smaller-the-Better) which is 182.84 dB. Also, the level values for each process parameter is plotted. Referring to the graphs, from the left, the slopes correspond to the Halo Implantation (Factor A), followed by S/D implantation (Factor B), Compensation Implantation (Factor C) and lastly V_{th} Adjust Implantation (Factor D) respectively.

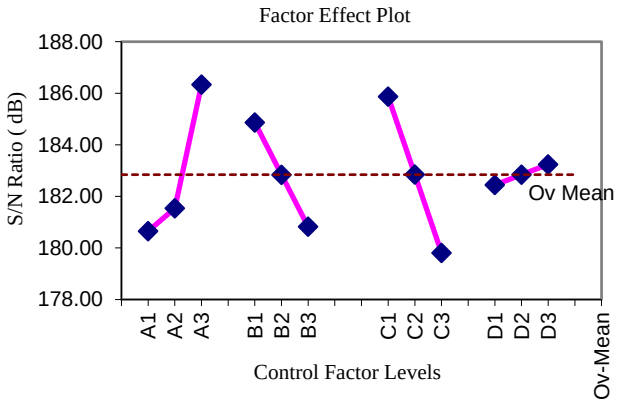


Figure 4 Factor effect plot for SNR (Smaller-the-Better)

3.3 Analysis of Variance (ANOVA)

The analysis of variance (ANOVA) is a common statistical analysis technique to determine the contribution of each process parameter by referring to the factor effect percentage. In the same time it can be used to investigate the process parameters that give the most effect to the device performance characteristics [19]. ANOVA consist of parameters like degree of freedom (DF), sum of squares (SS), mean square and factor effect percentage on SNR.

The result of ANOVA for the device is presented in Table 6. The factor effect percentage on SNR indicates the priority of a factor (process parameter) to reduce variation where the high percentage of a factor effect on SNR contributes to the greatest influence on the I_{LEAK}.

The results of the factor effect on the SNR clearly show that the Halo implantation dose has the most influence in minimizing the I_{LEAK} with 41%, followed by the Compensation Implantation with 40%. The percentage effect for the SNR for the S/D Implantation and V_{th} Adjust Implantation were much lower, being 18% and 1% respectively

Table 6 Results of ANOVA

	Process Parameter	Degree of Freedom (DF)	Sum of Square (SS)	Mean square	Factor Effect on SNR (%)
A	Halo Implantation	2	56	28	41
B	S/D Implantation	2	25	12	18
C	Compensation Implantation	2	55	28	40
D	V_{th} Adjust Implantation	2	1	0	1

4.0 CONFIRMATION RUN

Based on the results in Table 5 and also Figure 4, the highest SNR value of each process parameter level to achieve minimum I_{LEAK} can be discovered. For the Halo Implantation, the higher value is at level 3 with SNR of 186.34 dB, followed by S/D Implantation at level 1 with SNR of 184.87 dB, while Compensation Implantation at level 1 with SNR of 185.87 dB and last but not least is V_{th} Adjust Implantation at level 3 with SNR value of 183.24 dB. The best setting of the process parameters in the I_{LEAK} analysis is A_3, B_1, C_1, D_3 and this is summarized in Table 7. Finally, these parameters were then simulated with the noise factors to get the final I_{LEAK} results as noted in Table 8.

Table 7 Best setting of the process parameters

Symbol	Process Parameter	Level	Best Value (atom/cm^3)
A	Halo Implantation	3	$1.28e^{13}$
B	S/D Implantation	1	$5.10e^{13}$
C	Compensation Implantation	1	$3.65e^{13}$
D	V_{th} Adjust Implantation	3	$6.98e^{12}$

Table 8 Results of best setting parameter with added noises

LEAKAGE CURRENT (nA/µm)					SNR (STB)
I_{LEAK} 1 (X1,Y1)	I_{LEAK} 2 (X1,Y2)	I_{LEAK} 3 (X2,Y1)	I_{LEAK} 4 (X2,Y2)	I_{LEAK} (Mean)	
0.25295	0.26185	0.25331	0.26223	0.25759	191.78

After the optimization approach, the value of SNR (Smaller-the-Better) of the I_{LEAK} for the 22 nm n-type MOSFET device shows that it is in the range of the predicted SNR (Smaller-the-Better) where the range is between 189.81 dB and 192.97 dB. The lowest I_{LEAK} value obtained is 0.25295 nA/µm where the optimum noise factor was identified as 900°C for the PSG temperature and 850°C for the P-well Implantation annealing. The optimized device's final I_{LEAK} value is much lower than the maximum value predicted by ITRS 2011.

5.0 CONCLUSION

As a conclusion, the Taguchi method is a reliable technique in optimizing the process parameters in designing a 22 nm n-type MOSFET utilizing high-k/metal gate technology in order to achieve the optimum solution in the virtual fabrication with reference to the ITRS 2011. Leakage current was kept as minimum as possible to increase the speed performance. Using Taguchi method optimization, the best combination process

parameters and noise factors results a mean of I_{LEAK} value of 0.25759 nA/μm.

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