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DESIGN OF LOW POWER 8T SRAM WITH SCHMITT TRIGGER LOGIC

A. KISHORE KUMAR[1,*], D. SOMASUNDARESWARI[2], V. DURAISAMY[3], T. SHUNBAGA PRADEEPA[4]

[1]Hindusthan College of Engineering. & Technology, Coimbatore, India
[2]SNS College of Technology, Coimbatore, India
[3]Maharaja Institute of Technology, Coimbatore, India
[4]Coimbatore Institute of Technology, Coimbatore, India
*Corresponding Author: kishore_hindusthan@yahoo.in

Abstract

Static Random Access Memory (SRAM) has become a key element in modern VLSI systems. In this paper, a low power design of 8 Transistor SRAM cell with Schmitt Trigger (ST) logic is proposed. The main intention of this paper is to design a new SRAM cell architecture to reduce the power consumption during both read / write operations and to improve SRAM access stability. The proposed design is simulated using 0.18 μm process technology and compared with conventional 6T cell. Simulation results show that the proposed memory cell achieves significant improvements in power consumption during read and write operations. It can retain data at a lower supply voltage of 300 mV. This new type of SRAM design can operate at a maximum frequency of 1 GHz at 1 V supply voltage. These qualities of the proposed design make it a best choice for high performance memory chips in the semiconductor industry where reliability and power consumption are of great interest.

Keywords: VLSI, Low power, Memory, SRAM, Schmitt trigger.

1. Introduction

Over the past few decades, power reduction techniques in memory circuits have progressively geared up the list of researcher's design concerns, over the rising cost of energy, and an increasing sensitivity to green practices, low power consumption and the like, have become a major concern for design engineers.

Various classical approaches are proposed by the designers to reduce power consumption in memories. Power consumption in SRAM cell is considered one of the major issue in the high performance chips due to the popularity of battery operated electronic devices and mobile devices. The design of low-power SRAM is complex since it takes a large fraction of total power and die area in high-performance embedded processors. The leakage current of the memory is increased with the capacity such that more power will be consumed in the standby mode. Many schemes have been reported to improve the power consumption in memory devices, but reducing the leakage current is of great interest. In [1], a novel Schmitt trigger based differential 10-transistor SRAM bit cell suitable for subthreshold operation was proposed and achieved 18% reduction in leakage and 50% reduction in read/write power compared to the conventional 6T cell. In [2], fully-differential sub-threshold 10-transistors SRAM cell with auto-compensation was presented and achieved significant improvement in read and write SNM.

In [3], Ultra-low power digital subthreshold logic circuits were analyzed in both CMOS and Pseudo-NMOS logic families operating in the subthreshold region. In [4], a design of SRAM array in the subthreshold operation was proposed and performed a nominal analysis of power and stability. In [5], a sub-volt SRAM circuit scheme was presented to speed up the conventional low-voltage SRAM by more than a factor of two without applying excessive voltage and with maintaining the subthreshold leakage current to a tolerable level. In [6], an embedded high density 128 kb memory, utilizing a 5T single bit line SRAM cell was presented. In [7], a 7T SRAM cell was presented which depends on one of the bit lines during a write operation and achieved the write power consumption. In [8], stable SRAM cell design for the 32 nm node was proposed and demonstrated the smallest 6T and full 8T cells to date. In [9], a 256 kb sub-threshold SRAM operates below 400 mV was implemented in 65 nm CMOS technology which uses a 10T bit cell to enable sub-threshold functionality. In [10], the stability of both resistor-load (R-load) and full-CMOS SRAM cells was investigated analytically as well as by simulation.

In [11], the static noise margin (SNM) of 6T SRAM bit cells operating in sub-threshold was evaluated and analyzed the dependence of SNM during both hold and read modes on supply voltage, temperature, transistor sizes, local transistor mismatch due to random doping variation, and global process variation in a commercial 65 nm technology. In [12], a high-performance dual read port 32 nm 6T SRAM with one clock cycle access time and 8-way set associatively for low voltage applications is presented. In [13], a new SRAM cell architecture (9T Balanced type) which consists of an asymmetric inverter pair was proposed to reduce the power consumption. In [14], Schmitt trigger based SRAM using single ended input output transistors (7T) was proposed under 45nm CMOS technology to provide better read stability, write ability. In [15], Ultra Low Power 6T SRAM Using Adiabatic Technique is used for reduction of average power dissipation and it is reduced up to 75% using adiabatic technique and also shows the effect on static noise margin. In [16], a novel 7T SRAM cell is introduced and it is compared with the two existing 7T SRAM cells and achieved significant improvement in power consumption. In Fig. 1, different types of SRAM bit cells have been reported to improve the memory failure probability at a given supply voltage. 6T and 7T bit cells utilize differential read operation while 5T, 8T and

10T bit cells employ single ended reading scheme. 8T and 10T cells use an extra sensing circuit for reading the cell contents to achieve improved read SNM [1].

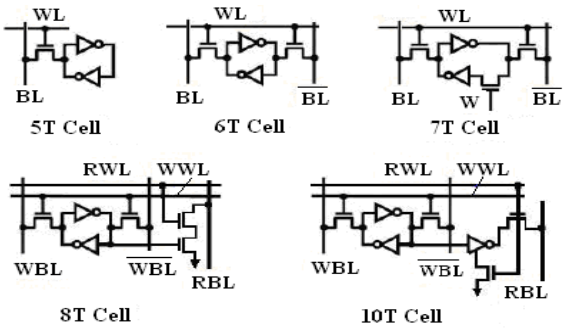

Fig. 1. Different SRAM Bit Cells [1].

In this paper, a low power design of 8 Transistor SRAM cell with Schmitt Trigger Logic (8T ST SRAM) is proposed to reduce the power consumption for complete operation with minimized operating leakage current.

2. Cell Design Concept

The proposed 8T ST SRAM cell design is shown in Fig. 2. The proposed design focuses on making the basic inverter pair of the memory cell effective for low voltage operations. The transistors P11, P12, P13, N11 forms one inverter pair and P21, P22, P23, N21 forms another inverter pair. The transistors N11 and N21 are also used as access transistors for the bit line. At low voltages, the cross-coupled inverter pair stability is of major concern during the transition and read operation, to improve the stability of data read (0 and 1), Schmitt trigger configuration is used. In this design, Schmitt trigger increases or decreases the switching threshold of an inverter depending on the direction (PX and NX) of the output transition. This adaptation is achieved with the help of series transistor feedback technique with reduced transistor count for the Schmitt trigger operation.

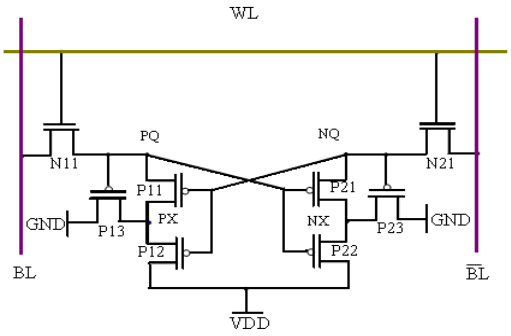

Fig. 2. Proposed 8T ST SRAM Cell.

2.1. Read and write operation

In read operation of the memory cell, the voltage divider of PMOS and NMOS changes PQ (Q) voltage. If this voltage is more than the other inverter pair, it causes data flip, resulting failure data. To overcome this problem, we need to increase threshold voltage on other inverter pair, vice versa for the storage of "0" and "1" at PQ (Q) and NQ (Q bar). This is achieved with the help of pass transistor feedback mechanism (P13, P23). It improves the threshold in both transitions at PX and NX points, which improves the overall stability of the cell and avoids data failure during read cycle. If BL and BL bar is at zero potential, circuit turns to read mode. During the read mode, positive edge trigger in WL line enables the stored output potential "1 or 0" in the combined Q and Q bar lines. In case of write operation, BL and BL bar act as the input lines for the given data. For read operation BL and BL bar act as the control lines, Q and Q bar act as the data output lines. It enables to read the bits without any error even at lower supply voltages. For the better usability and to reduce read / write lines, Q and Q bar can be connected with the same BL and BL bar with some driver circuits. The read and write operation of the proposed 8T ST SRAM cell design is summarized in Table 1.

The schematic diagram of 8T ST SRAM cell is shown in Fig. 3. The various metrics of the proposed 8T ST SRAM cell design is compared with the existing 5T, 6T, 7T, 8T and 10T SRAMs and presented in Table 2 [1].

Table 1. Read / Write Operation of the Proposed 8T ST SRAM Cell Design.

Operation	BL	BL bar	WL	PQ (Q)	NQ (Q bar)	Operation	BL
Write ("1")	1	0	⎍	1	0	Write ("1")	1
Write ("0")	0	1	⎍	0	1	Write ("0")	0
Read	0	0	⎍	Stored output	Stored Output	Read	0

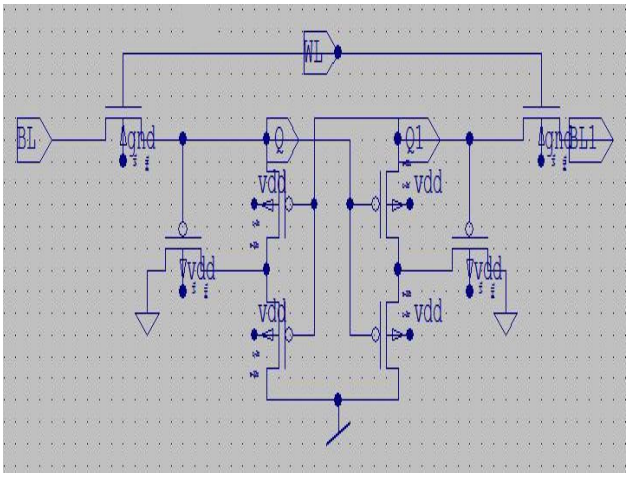

Fig. 3. Schematic of 8T ST SRAM Cell.

Table 2. Comparison of SRAM Bit Cells.

Metrics	5T	6T	7T	8T	10T	Proposed
Read	Single	Differential		Single Ended		Differential
#WL	1	1	1	2	2	1
#BL	1	2	2	3	3	2
#NMOS in	2	2	2 or 3	2	3	2
#PMOS	2	2	2	2	3	6

3. Simulation Results and Discussion

The simulation results of 8T ST SRAM cell design for read / write operation of data "1" is shown in Fig. 4 and read / write operation of data "0" is shown in Fig. 5. Tanner EDA tool with SPICE support is used for simulation using 0.18 µm process technology.

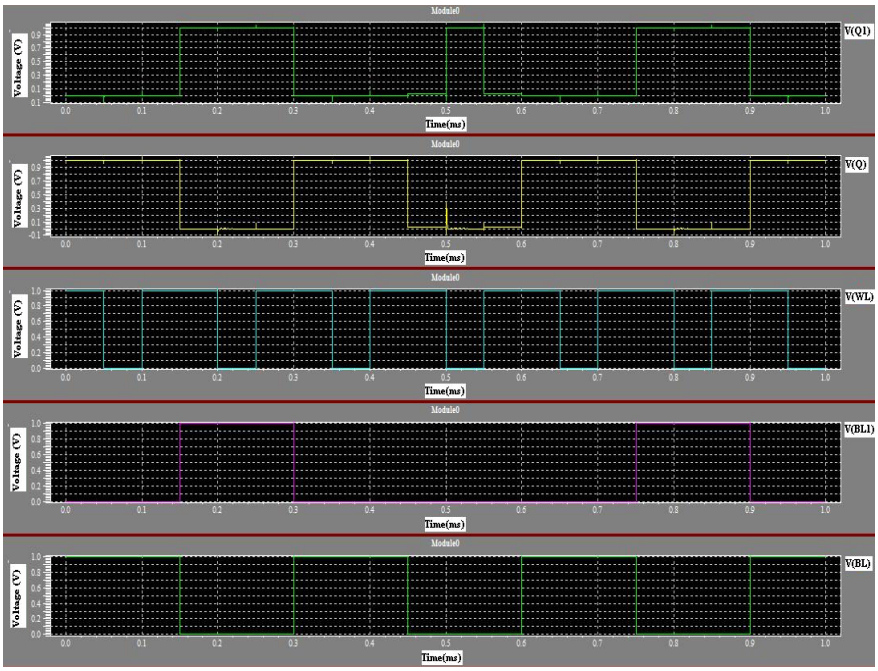

Fig. 4. Simulation Results for Read / Write Operation of Data "1".

In the proposed 8T ST SRAM cell design, the power consumption during read "0" is small as compared to the conventional designs due to no transition during read "0".

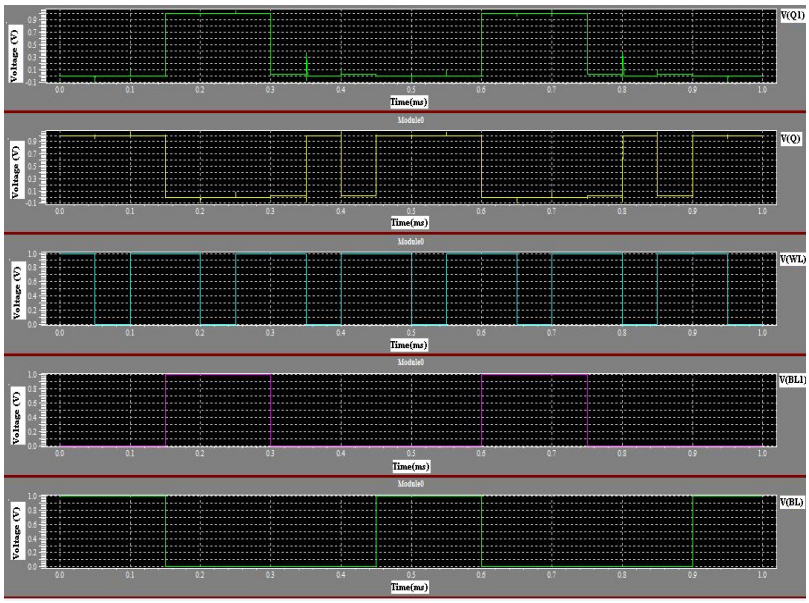

Fig. 5. Simulation Results for Read / Write Operation of Data "0".

The proposed design consumes less power than conventional 6T, 7T SRAM and adiabatic SRAM during write/read operation, reported in Table 3. This significant improvement in power consumption of 8T ST-SRAM is achieved due to reduction in leakage current of this circuit. The average power consumption during write (0/1) operation of the proposed 8T ST SRAM cell design is compared with conventional 6T, 7T SRAM and adiabatic SRAM, listed in Table 4. The power comparison graph for read and write operation is shown in Fig. 6.

Table 3. Average Power Consumption during Write/Read.

SRAM Types	Average power (µW)
6T Conventional	14.6
7T SRAM [16]	3.316
Adiabatic SRAM [15]	2.22
Proposed Design (8T ST SRAM)	1.6

Table 4. Average Power Consumption during Write '0'/'1'.

SRAM Types	Average power (µW)
6T Conventional	15.9
7T SRAM [16]	3.135
Adiabatic SRAM [15]	2.07
Proposed Design (8T ST SRAM)	1.734

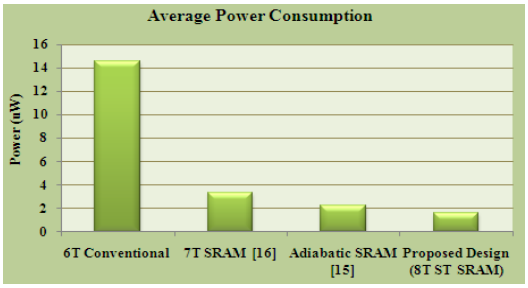

Fig. 6. Average Power Consumption during Write/Read Operation.

4. Conclusions

In this paper we have revealed a novel methodology for designing a low power design of 8 Transistor SRAM cell with Schmitt Trigger Logic (8T ST SRAM). The performance of this design is compared with the existing techniques. The power consumption of the proposed memory cell reduces drastically for complete operation. This significant improvement in power consumption of 8T ST-SRAM is achieved due to reduction in leakage current of this circuit. The proposed 8T ST SRAM can retain data at a lower supply voltage of 300 mV. This new type of SRAM design can operate at a maximum frequency of 1 GHz at 1V supply voltage. The proposed design is simulated using 0.18 µm process technology and compared with conventional 6T cell. This approach confirms the feasibility of SRAM circuits in low power applications. In view of these, it is concluded that the proposed design is best fit for microprocessor applications where low power and SRAM access stability are of critical design considerations.

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