Characterization & Optimization of 32nm P-Channel MOSFET Device

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***Abstract*— In this paper, effect of the process parameters variation on response characteristics such as threshold voltage (V_{TH}) in 32nm p-channel Metal-Oxide Semiconductor Field Effect Transistor (MOSFET) device was investigated. An orthogonal array, signal-to noise (S/N) ratio and analysis of variance were employed to study the performance characteristics of the p-channel device. The control factors were used in this research are oxide growth temperature, V_{TH} implant energy, Source/Drain (S/D) implant dose and compensation implant energy. The fabrication of the transistor device was performed using TCAD simulator, consisting of a process simulator, ATHENA and device simulator, ATLAS. The results were then subjected to the Taguchi method to determine the optimal process parameters and to produce predicted values. In p-channel device, V_{TH} implant energy (57%) was identified as one of the control factor that has the strongest effect on the threshold voltage. The result shows that the V_{TH} value has least variance and percent different from the target value (-0.289V) for this device is 3.11% (-0.280V). As conclusions, setting up design of experiment with the Taguchi Method of L_9 orthogonal arrays and TCAD simulator, the optimal solution for the robust design recipe of 32nm p-channel device was successfully achieved.**

Key words – threshold voltage, p-channel, L_9 orthogonal array, Taguchi Method.

I. INTRODUCTION

METAL Oxide Semiconductor Field Effect Transistor (MOSFET) devices need to have good performance with low cost and low power dissipation. The most effective way to enhance performance and reduce costs is to scale the device gate length and gate oxide. Scaling the gate length results in fabricating more devices per wafer and thus reduce the cost per chip, while scaling the gate oxide enhances the drive current and reduces the short channel effects due to gate length scaling [1,2]. However, as the gate oxide becomes thinner, the power to operate transistor increases because of greater gate oxide leakage current. The size reduction of the channel length MOSFET also makes a great enhancement to MOSFET operation [3,4]. Today, metal-oxide semiconductors (MOS) are process invariability use ion implantation into the channel region, which alter the doping profile near the surface of silicon substrate. The ion implantation procedure provided much more accurate to control doping than the diffusion [5].

The most significant physical parameter's MOSFET in this process is the threshold voltage (V_{TH}). V_{TH} is the minimum gate voltage required to produce a channel between source and drain. It is able to define as the minimum voltage for strong inversion to arise [6]. Many researchers have introduced the technique to control the electrical characteristics, especially threshold voltage and saturation current and also to optimize the process of parameters variation [7]. In design of devices with deep sub-micron technology, the analysis of variability has become a highly essential tool, to forecast the response of variation at early stage in the design cycle due to process parameter spreads. The variation will impact the performance of a device. It may show wider variability leading to the degradation of yield in recent technologies and applications [7,8]. In this project, to identifying MOSFET process parameters, whose variability will impact almost of the device characteristics is realized by using Taguchi method.

II. EXPERIMENT DESCRIPTION

The process modules start with wafer preparation, followed by well formation, isolation formation, transistor making and interconnection as shown in Figure 1 [9]. The wafer preparation includes epitaxial silicon growth, wafer clean and alignment mark etch. Well formation defines the substrate type for PMOS transistor. Transistor making involves gate oxide growth, polysilicon deposition, photolithography, polysilicon etch, ion implantation and thermal annealing. These are the most crucial process steps in the IC processing sequence [10,11]. The substrate used for the experiment was a p-type (boron doped) silicon wafer with <100> orientation. Then it was followed by growing an oxide layer on top of the silicon bulk using dry oxygen at a temperature of 970^{o}C for 20 minutes. N-wells are created starting with developing a 200Å oxide screen on the wafers followed by phosphorus doping. The oxide layer was etched after the doping process was completed. It was followed by annealing process to strengthen the structure. The process was done at 950^{o}C for 100 minutes in a nitrogen environment, and followed by dry oxygen for 36 minutes in order to ensure that boron atoms were spread properly in the wafer. The masking oxide then was etched. The next step was to produce a Shallow Trench Isolation (STI) of 350Å thickness. In order to form STI layer, the wafer was oxidized in dry oxygen for 25 minutes at 900^{o}C. Then, a

1500Å nitride layer was deposited on the top of the oxide layer by applying the Low-Pressure Chemical Vapour Deposition (LPCVD) process. This thin nitride layer was acted as the mask when silicon was etched to expose the STI area. Photo resistor layer with the thickness of 1.0µm was then deposited on the wafers and unnecessary part will be etched using the Reactive Ion Etching (RIE) process. An oxide layer was grown on the trench sides to eliminate any impurity from entering the silicon substrate. Chemical Mechanical Polishing (CMP) was then applied to eliminate extra oxide on the wafers.

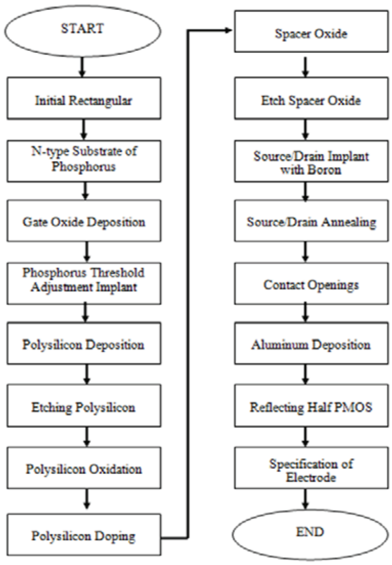

Figure 1: Processing Steps for Build MOSFET Structure

Lastly, STI was annealed for 15 minutes at 900°C temperature. A sacrificial oxide layer was then grown and etched to eliminate defects on the surface. Next process was to growth the gate oxide layer. In order to achieve this, the silicon wafer was oxidized in dry oxygen at 820ºC for short time at 100ms. The short time is needed to ensure a very thin layer and not more than 1.1nm of oxide thickness was grown [8,12]. The V_{TH} adjust implantation was performed to implant Boron Difluoride (BF2) at N-well active area in order to adjust the V_{TH} of the device. The polysilicon was then deposited on the top of the wafer and then etched accordingly to produce the gate contact point desired. Halo implantation then took place in order to get an optimum performance device. phosphorus with a dose of $2.55\text{x}10^{13}$atom/cm^3 and with energy of 159keV tilted at 20º was performed in PMOS device. The dosage was varied in order to get the optimum value. A nitride layer was then deposited on top of the polysilicon gate and immediately etched to expose the top surface of the silicon layer. Sidewall spacers were developed after that process. Due to the nature of the substrate surface at the gate, side wall spacers of 0.0867µm thickness were created. These were used as a mask for source and drain implantation. Next, source-drain implantation was done using boron with the dose of $6.9\text{x}10^{13}$ atom/cm^3 at 12keV implantation energy and this was tilted 7º. Boron atoms were implanted at a desired concentration to ensure the smooth current flow in PMOS device. A cobalt silicide layer of 0.0867µm was then deposited on top of the substrate and then was annealed by a rapid thermal annealing process in a nitrogen environment at 900°C. Immediately after, the residual area of cobalt was etched away. The next process was the development of a 0.3µm BPSG layer. This layer will be acted as Premetal Dielectric (PMD), which is the first layer deposited on the wafer surface when a transistor was produced. This transistor was then connected with aluminium metal. After this process, the second aluminium layer was deposited on the top of the Intel Metal Dielectric (IMD) and unwanted aluminium was etched to open the contacts. The procedure was completed after the metallization and etching were performed for the electrode formation, and the bonding pads were opened. Once the devices were built with ATHENA, the complete devices can be simulated in ATLAS to provide specific characteristics such as the Id versus Vg curve. The threshold voltage (V_{TH}) can be extracted from that curve [9,13].

A. Taguchi Orthogonal L_9 Array Method

With Taguchi method, the desired design is finalized by selecting the best performance under given conditions. The main tool used in the Taguchi method is the orthogonal array (OA) [14,15]. In this research, an L_9 OA which has 9 experiments was used. Each row of the OA comprises a single experiment with a particular set of control factor levels followed at the end by all combinations of selected noise factors. The two noise factors will create four set of experiments consisting of 36 runs. A four set of L_9 orthogonal array runs, is the minimum number of results needed for this project analysis. The values of the process parameter and noise factor at the different levels are listed in Table 1 and Table 2 respectively.

Table 1: Control factor parameters

Symbol	Process Parameter	Units	Level 1	Level 2	Level 3
A	Oxide growth temperature	°C	820	822	824
B	V_{TH} implant energy	keV	4.5	5.0	5.5
C	S/D implant dose	atom cm^{-3}	6.45e13	6.50e13	6.55e13
D	Compensation implant energy	keV	2.6e13	2.8e13	3.0e13

Table 2: Noise factor parameters

Symbol	Noise factor	Units	Level 2	Level 3
X	PSG temperature	^{o}C	900	901
Y	Etch cobalt temperature	^{o}C	910	915

III. Result and Discussion

The results of threshold voltage (V_{TH}) were analyzed and processed with Taguchi Method to get the optimal design. The optimized results from Taguchi Method were simulated in order to verify the predicted optimal design.

A. Analysis of 32nm PMOS Device

Nine experiments of L_9 array were conduct which each contains four sets of experiments. The completed response for V_{TH} data is shown in Table 3. After nine experiments of L_9 array have been done, the next step is to determine the control factor parameters that can gave more effect to the device characteristics. Signal-to-noise (S/N) ratio was used to find out the optimal process parameters and analyze the experimental data. The S/N ratio for each level of the process parameters is computed based on S/N analysis.

Table 3: The experimental results of V_{TH}

Experiment No.	Threshold Voltage, V_{TH}(V)			
	$V_{TH}(X_1Y_1)$	$V_{TH}(X_1Y_2)$	$V_{TH}(X_2Y_1)$	$V_{TH}(X_2Y_2)$
1	-0.2866	-0.2864	-0.2941	-0.2939
2	-0.3448	-0.3447	-0.2958	-0.2956
3	-0.3906	-0.3905	-0.3902	-0.3900
4	-0.3780	-0.3778	-0.3778	-0.3776
5	-0.2646	-0.2644	-0.2617	-0.2615
6	-0.3889	-0.3888	-0.3888	-0.3886
7	-0.2428	-0.2426	-0.2457	-0.2455
8	-0.4333	-0.4331	-0.4286	-0.4284
9	-0.3117	-0.3115	-0.3126	-0.3124

In this research, V_{TH} of the 32nm p-channel (PMOS) device belongs to the nominal-the-best quality characteristics. This S/N Ratio (SNR) is used to get the V_{TH} value closer or equal to a given target value (-0.289V) based on ITRS 2011 [16]. In the nominal-the-best, there are two types of a factor to find, which are dominant and adjustment factors. The S/N ratios for the device are calculated and listed in Table 4.

Table 4: Mean, variance and S/N ratio for PMOS device

Exp. No.	Mean	Variance	SNR (Mean)	SNR (Nominal-the-best)
1	0.290	1.88e-05	-10.7	36.5
2	0.320	8.02e-04	-9.89	21.1
3	0.390	7.58e-08	-8.17	63.0
4	0.378	2.67e-08	-8.45	67.3
5	0.263	2.82e-06	-11.6	43.9
6	0.389	1.58e-08	-8.21	69.8
7	0.244	2.82e-06	-12.2	43.3
8	0.431	7.38e-06	-7.3	44.0
9	0.312	2.83e-07	-10.1	55.4

The effect of each process parameter on the S/N ratio at different levels can be separated out because the experimental design is orthogonal. The S/N ratio for each level of the process parameters is summarized in Table 5. In addition, the overall mean S/N ratio for the nine experiments is also calculated.

Table 5: S/N ratio responses for the threshold voltage

Symbol	Process Parameter	SNR (Nominal-the-Best)			Total Mean SNR
		Level 1	Level 2	Level 3	
A	Oxide growth temperature	40.21	60.33	47.54	49.36
B	V_{TH} implant energy	49.02	36.33	62.73	
C	S/D implant dose	50.11	47.90	50.06	
D	Compensation implant energy	45.26	44.71	58.11	

Figures 2 and 3 show the S/N ratio and means graphs respectively for 32nm PMOS device. Basically, the larger of the S/N ratio (SNR), the quality characteristic of threshold voltage is better [17,18].

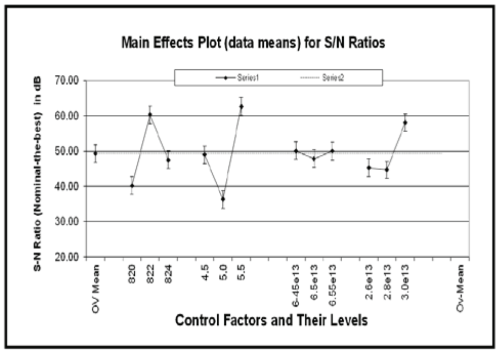

Figure 2: S/N Ratios Graph for V_{TH}

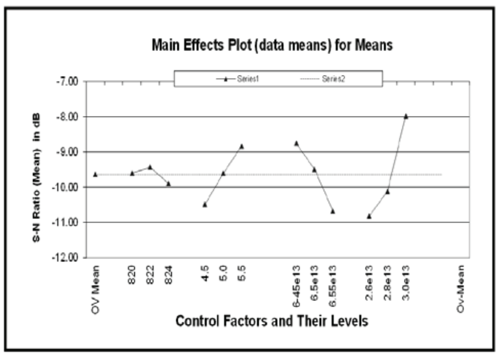

Figure 3: Means Graph for V_{TH}

B. Analysis of Variance (ANOVA)

The purpose of the analysis of variance (ANOVA) is to investigate which of the device parameters significantly affect the performance characteristics. It calculates parameters known as sum of squares (SSQ), mean square (MSSQ), degree of freedom (DF), variance, F-value and percentage of each factor. The result of ANOVA for the PMOS device is presented in Table 6.

Table 6: Results of ANOVA for PMOS device

Symbol	Process Parameter	DF	SSQ	MSSQ	Factor Effect on SNR (%)	Factor Effect on Mean (%)
A	Oxide growth temperature	2	622	311	31	1
B	V_{TH} implant energy	2	1046	523	52	18
C	S/D implant dose	2	10	5	0	24
D	Compensation implant energy	2	345	172	17	57

According to this analysis, the most dominant factors for S/N Ratio are factor B (V_{TH} implant energy – 52%) and factor A (Oxide growth temperature – 31%). Therefore, these factors should be set at 'best setting' and cannot be used as an adjustment factors. Whereas factor D (Compensation implant energy) was described as an adjustment factor because it has the large effect on mean (57%) and small effect on variance (17%) if compare with other factors. The analysis of average performance showed that the optimum condition is A2,B3,D1. Because factor C (S/D implant dose) was found not significant (pooled - 0%) in threshold voltage, there could be set at any level [17]. The full recommendation for optimization is A2,B3,C3,D1 i.e. oxide growth temperature at level 2, V_{TH} implant energy at level 3, S/D implant dose at level 3 and compensate implant dose at level 1. Figures 4 and 5 show the pareto analysis of effect with parameter V_{TH} (PMOS) from other researchers using L_{18} OA Taguchi Method [4] and Response Surface Methodology (RSM) [19] respectively. According to these figures, it can be seen that V_{TH} implant energy has an influential role on the threshold voltage of the device.

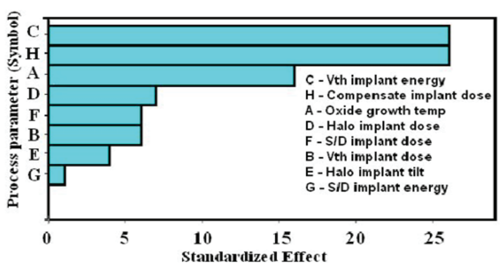

Figure 4: Pareto plot for PMOS using L18 OA Taguchi Method

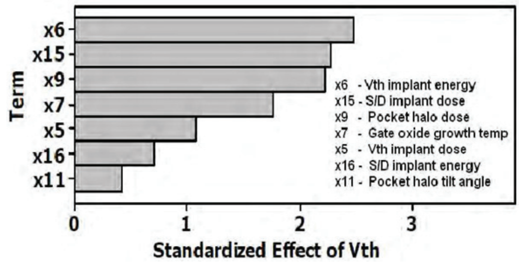

Figure 5: Pareto plot for PMOS Device using RSM

C. Confirmation Test

The confirmation test is used to verify the estimated result with the experimental results. Best setting of the process parameters for PMOS device that had effects on V_{TH} which had been suggested by Taguchi Method is shown in Table 7. In here, the confirmation test was required in PMOS device because the optimum combination of parameters and their levels i.e. A2,B3,C3,D1 did not correspond to any experiment of the orthogonal array. The result of the final simulation for this device is shown in Table 8.

Table 7: Best setting of the process parameters

Symbol	Control Parameter	Units	Best Value
A	Oxide growth temperature	^{o}C	822
B	V_{TH} implant energy	keV	5.5
C	S/D implant dose	atom cm^{-3}	$6.55x10^{13}$
D	Compensation implant energy	keV	$2.6x10^{13}$

Table 8: Results of confirmation experiment for V_{TH}

Threshold Voltage (Volts)				SNR (Mean)	SNR (Nominal-the-Best)
X_1Y_1	X_1Y2	X_2Y_1	X_2Y_2		
-0.2798	-0.2796	-0.2797	-0.2795	-11.10dB	66.7dB

Before the optimization approaches, the best S/N ratio (Nominal-the-best) is 67.3dB at row of experiment no. 4 (Please refer Table 4). Whereas the variance is 0.163mV and mean for threshold voltage is -0.378V. The percent different of this threshold voltage value from the nominal value, -0.289V [16] is higher (30.8%).

After the optimization approaches, the S/N Ratio (Nominal-the-best) and S/N Ratio (Mean) of threshold voltage for PMOS device are 66.7 dB and -11.1 dB respectively. These values are within the predicted range. For S/N Ratio (Nominal-the-best), 66.7 dB is within predicted range S/N ratio of 74.60 to 64.61 dB (69.60 ± 5.0dB). While for S/N Ratio (Mean), -11.1 dB is within predicted range S/N ratio of -6.05 to -16.04 dB (-11.05 ± 5.0 dB). These show that Taguchi Method can predict the optimum solution in finding the 32 nm PMOS fabrication recipe with appropriate threshold voltage value.

The variance and mean for threshold voltage after optimization approaches are 0.129mV and 0.280V respectively. It can be shown that the variance is slightly decrease from the previous value (0.163mV) and threshold voltage value is also closer to the nominal value (target). The V_{TH} value after the optimization approach is just 3.11% different from the target. Table 9 shows the simulated values versus ITRS 2011 prediction for V_{TH} in 32nm PMOS device.

Table 9: Simulation versus ITRS 2011 Prediction

Device	Simulation	ITRS 2011 Prediction [16]
PMOS	-0.280V	-0.289V

It is clearly shown that our design simulation is closer to International Technology Roadmap for Semiconductor (ITRS) 2011 prediction [16]. The closer the quality characteristic value to the target, the better the product quality will be [18].

IV. Conclusion

Through this paper, the main factors that affect the response characteristics of 32nm PMOS device was found, together with the optimal factor levels. There were shown that V_{TH} implant energy and oxide growth temperature were identified as the most dominant or significant factors for S/N Ratio in PMOS device. While compensation implant dose was identified as an adjustment factor in this device. The adjustment factor has been used to get the nominal (target) value of threshold voltage for PMOS device closer to -0.289V. The percent different of threshold voltage value from the target after the optimization approach is just 3.11%. This value is closer with International Technology Roadmap for Semiconductor (ITRS) 2011 prediction. It can be shown that the optimum solution in achieving the desired transistor was successfully predicted by using Taguchi Method.

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