

Application of Taguchi Method in Optimization of Shallow PN Junction Formation

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Abstract—In this research, optimization of shallow PN junction formation through dopant diffusion from Spin on Dopant (SOD) in Ultra Large Scale Integrated (ULSI) technology by using taguchi method was investigated. The shallow junction formation by using the polysilicon/Si structures has the advantages of lower sheet resistance in comparison with the conventional Si junction. Boron and phosphorus diffusion into silicon from SOD sources has been investigated using conventional furnace and rapid thermal diffusion. Diffusivity of boron in SOD was found to be much faster than in the normal oxide, and it was slower in the Si. Process simulation for shallow PN junction was used Silvaco TCAD Tools. The shallow PN junction with junction depth below than 30nm has been produced using rapid thermal diffusion. From the simulation result, the value of Sheet resistance (Rs) and Junction depth (Xj) were analyzed by using L₁₈ orthogonal array (OA) in Taguchi Method. Control factors that were used namely material, time and temperature. The analysis of variance shows the process parameter of material, and temperature is significant based on 95% confidence level towards junction depth and sheet resistance respond in the shallow PN junction device. So that the junction depth and sheet resistance decreased follows the material and temperature. As conclusion, taguchi method can be utilized to find optimum solution in fabricating to get a good performing device.

Index Terms— Shallow PN Junction, Taguchi Method, Silvaco TCAD, Spin on Dopant, Spin On Glass.

I. INTRODUCTION

THE most recent development in the electronic world is the production of the small electronic device and smart. By decreasing the device feature size, it will reduce the cost for manufacturing and also provide improvement. Silicon technology has played a major role in sustaining the semiconductor industry growth [1]. The concept of device scaling in silicon transistor has consistently resulted in better device density and performance [2]. Production of small components that result from the formation of a P-N junction is basically using Spin On Glass (SOG) techniques. Spin on Glass also called as Spin On Dopant (SOD) for the deep sub-micron devices for the future of the ULSI. With the advantages of no transient enhanced diffusion and no metal contamination, the diffusion from highly doped SOG is a good technology for the shallow p-n junction formation [3, 4]. The process of absorption of boron and phosphorus into silicon

from SOD resources will be explored. This project was used conventional furnace diffusion. The diffusion process from SOD was simulated as diffusion from a doped oxide source by using the equilibrium diffusion model. Diode realization will be carried out for the electrical characterization of these junctions.

PN Junction can be fabricated using multiple methods. However, diffusion is still a dopant method that mostly used in discrete semiconductor fabrication and monolithic integrated circuit. Diffusion is the movement of impurity atoms at the surface of the silicon into the bulk of silicon. It is the process of doping the silicon to introduce impurities. Diffusion takes places from higher concentration to lower concentration. Diffusion is done at very high temperatures above 10000°C. In general, diffusion is good for heavy doping and creating deep junctions. Ion Implantation is the process by which impurity ions are accelerated to a high velocity and physically lodged into the target material [5, 6]. Annealing is required to activate ions. In order to implement this research, the software Silvaco TCAD Tools was used to format a shallow P-N Junction diode [7].

Dr. Genichi Taguchi was the person who introduced the Taguchi Method as early as 1980. Taguchi Method has six steps, which are problem identification, brainstorming session, an experimental design, run experiment, then analyze result and confirmation runs [8, 9]. These facts were verified by using three of Signal-to-Noise ratios (SNR) such as smaller-the-better, larger the better and nominal-the-best. In this research, sheet resistance (Rs) and junction depth (Xj) of the Shallow PN junction device belongs to the smaller-the-best quality characteristics. Taguchi Method involves an analysis that reveals which of the factors are most effective in reaching the goals and the directions in which these factors should be adjusted to improving and optimizing the result [9, 10]. Taguchi method uses special design orthogonal arrays to study the entire process parameter space with only a small number of experiments. The orthogonal array helps preserve the consistency of design, even though different researchers may assign different factors and with different columns [11].

II. METHODOLOGY

For electrical characterization of P-N junctions, diodes were realized using different active windows. In order to form P-N junctions, the conventional furnace was used to diffuse SOD layer into silicon. Firstly, the size of junction that will be fabricated were declared before the next fabrication process with declaring 'mesh' in the first step of the program. Smaller value of mesh made the time taken to process the simulation longer. In this project, silicon with resistivity of $8\Omega/\text{cm}^2$ and orientation of $\langle 100 \rangle$ were used. Then the n-type silicon wafer has been formed after doping the phosphorus.

Next, the SOD- B150 Layer with 400 A was deposited onto the formed wafer. The oxide layer which contains boron as impurities was obtained from ATHENA for SOD- B150 layer model, and the selected boron density was $7 \times 10^{21} \text{ion}/\text{cm}^3$. The commands to get simulated profile are almost same with SRP profile which some of the parameters in the doped oxide diffusion model were changed. These parameters are boron layer model diffusion into SOD (oxide) and boron diffusion into silicon [12]. For boron diffusion in SOD layer, half factor value (DIX.O) and activation energy (DIX.E) were changed while boron diffusion in silicon divided into two, which are intrinsic diffusion for neural vacancies and intrinsic diffusion for single positively charged vacancies. The intrinsic diffusion for neural vacancies not affected the simulated diffusion profile, and its value never changed. The intrinsic diffusion for single positively charged vacancies was very important, especially for diffusion with high boron density [7, 4].

The deposited wafer by SOD-B150 layer was put into the conventional furnace in 900°C within ten minutes in nitrogen ambient. Then, the SOD-B150 layer was etched out until no SOD-B150 layer left inside after the previous process [13, 14]. Finally, the 'extract' commands were written to obtain several important parameters such as the depth of junction (X_j), Sheet Resistance (R_s) and SRP profile graph for silicon wafer, which has diffused with SOD- B150. The 'extract' commands were display all the values. All the process showed in codes was repeated in different files with different temperature such as 850°C , 900°C and 950°C within same times which are 15 minutes, 30 minutes and 45 minutes.

A. Taguchi Method L_{18} Orthogonal Array (OA)

In this research, an L_{18} orthogonal array in taguchi method which has eighteen experiments are being used. Table 1 shows the values of the process parameter at the different levels. There are only three process parameters (control factors) was used for this experiment. The control factors are material, time and temperature. The material was varied for 2 levels while the time and temperature were varied for 3 levels. Table 2 shows the experimental layout using L_{18} OA. Eighteen different experiments in the Shallow PN junction device were performed using the design parameter combinations in the specified orthogonal array table. Four specimens were simulated for each of the parameter combinations.

Table 1: Process parameters and their levels

Symbol	Process Parameter	Unit	Level 1	Level 2	Level 3
A	Material	-	Boron	Phosphorus	-
B	Time	Minute	15	30	45
C	Temperature	Celsius	850	900	950

Table 2: Experimental Layout using L_{18} Orthogonal Array

Exp. No.	Process Parameter Level		
	A (Material)	B (Time)	C (Temperature)
1	1	1	1
2	1	1	2
3	1	1	3
4	1	2	1
5	1	2	2
6	1	2	3
7	1	3	1
8	1	3	2
9	1	3	3
10	2	1	1
11	2	1	2
12	2	1	3
13	2	2	1
14	2	2	2
15	2	2	3
16	2	3	1
17	2	3	2
18	2	3	3

III. RESULTS AND DISCUSSIONS

Simulation was done by using ATLAS and ATHENA modules in Silvaco TCAD tools. ATHENA was used to generate PN Junction structure with doping area. Graph to display values of Sheet resistance (R_s) and Junction resistance (X_j) is gained from ATLAS module. The data of R_s and X_j from simulation will be applied to the taguchi method to get the best value. In this project, the L_{18} orthogonal array (OA) was used to analyze the value of R_s and X_j to get the optimal design. The optimized results from Taguchi Method were simulated in order to verify the predicted optimal design.

A. Result of R_s and X_j for shallow PN Junction device

Fig. 1 shows the PN Junction Structure. Fig. 2 shows the SRP Doping Vs Depth. The value for X_j is below 30nm. The value is about 25nm.

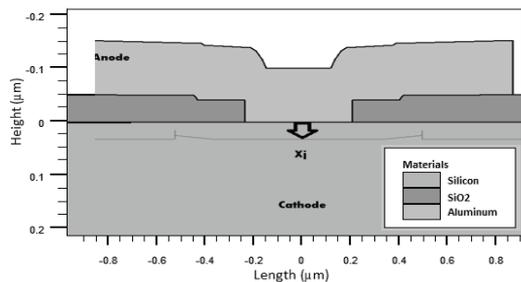


Figure 1: PN Junction Structure

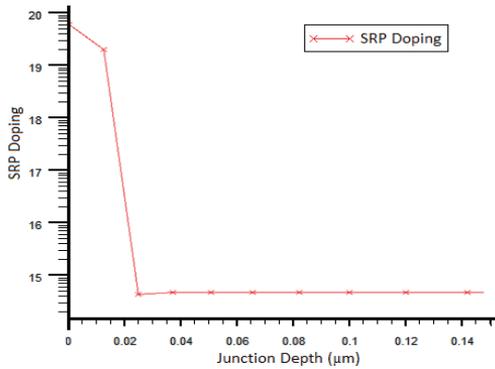


Figure 2: The SRP Doping Vs Depth.

Tables 3 and 4 show the fifty-four simulation values of Rs and Xj respectively. Besides three control factors, there are two types of noise factors, which are oxide diffusion temperature unit and oxide diffusion time. Each of the noise factors was varied for two levels to get four readings of Rs for every row of experiment.

Table 3: Result of Rs for Shallow PN junction

Experiment no.	Sheet Resistance (Rs)			
	Rs1(U1V1)	Rs2(U1V2)	Rs3(U2V1)	Rs4(U2V2)
1	1792.2	1880.96	1779.46	1786.67
2	512.29	513.445	510.602	511.559
3	170.795	170.98	170.524	170.678
4	1168.75	1172.83	1162.81	1166.18
5	345.682	346.229	344.88	345.335
6	116.85	116.939	116.72	116.794
7	919.479	922.101	915.652	917.821
8	275.548	275.902	275.029	275.323
9	93.8652	93.923	93.7804	93.8285
10	2758.74	2759.05	2758.28	2758.54
11	253.435	253.466	253.39	253.415
12	41.0597	41.0644	41.0527	41.0567
13	727.251	727.334	727.129	727.198
14	97.2832	97.2949	97.266	97.2757
15	13.3889	13.3903	13.3869	13.388
16	441.179	441.231	441.103	441.147
17	51.1719	51.1778	51.1631	51.1681
18	7.46063	7.46139	7.4595	7.46014

After eighteen experiments of L₁₈ array have been done, the next step is to determine, which control factors can give the effect to a device characteristics. Signal-to-noise (S/N) ratio was used to easily find out the optimal combinations. In this research, Rs and Xj of the Shallow PN junction device belongs to the smaller-the-best quality characteristics. The S/N Ratio (SNR) for each experiment in this device can be expressed as [8, 9]:

$$\eta = 10 \text{Log}_{10} \left[\frac{1}{n} \sum (Y_1^2 + Y_2^2 + \dots + Y_n^2) \right] \quad (1)$$

Table 4: Result of Xj for Shallow PN junction

Experiment no.	Junction Depth (Xj)			
	Xj1(U1V1)	Xj2(U1V2)	Xj3(U2V1)	Xj4(U2V2)
1	29.6975	29.6402	29.7817	29.7339
2	60.2257	60.1684	60.3099	60.2621
3	125.83	125.773	125.914	125.867
4	40.1629	40.1056	40.2471	40.1993
5	85.4651	85.4071	85.5493	85.5015
6	178.057	177.999	178.141	178.093
7	47.332	47.2747	47.4162	47.3684
8	104.132	104.075	104.216	104.168
9	218.07	218.013	218.155	218.107
10	462.998	462.941	463.082	463.034
11	581.467	581.41	581.551	581.504
12	706.627	706.57	706.711	706.664
13	515.461	515.404	515.545	515.498
14	641.909	641.851	641.993	641.945
15	825.95	825.893	826.034	825.986
16	545.062	545.005	545.146	545.098
17	684.762	684.704	684.846	684.798
18	918.082	918.024	918.166	918.118

Where n is the number of tests and Y_i the experimental value of the Rs or Xj. By applying Eqn. 1, the S/N Ratio, η for each experiment in Shallow PN junction device was calculated and given in Table 5.

Table 5 Mean and S/N ratio using the value of Rs and Xj

Exp. No.	Mean Sum of Squares	SNR (Smaller-the-better, dB)	Mean Sum of Squares	SNR (Smaller-the-better, dB)
1	3.3E+06	-65.15	8.8E+02	-29.46
2	2.6E+05	-54.18	3.6E+03	-35.60
3	2.9E+04	-44.65	1.6E+04	-42.00
4	1.4E+06	-61.35	1.6E+03	-32.08
5	1.2E+05	-50.77	7.3E+03	-38.64
6	1.4E+04	-41.35	3.2E+04	-45.01
7	8.4E+05	-59.26	2.2E+03	-33.51
8	7.6E+04	-48.80	1.1E+04	-40.35
9	8.8E+03	-39.45	4.8E+04	-46.77
10	7.6E+06	-68.81	2.1E+05	-53.31
11	6.4E+04	-48.08	3.4E+05	-55.29
12	1.7E+03	-32.27	5.0E+05	-56.98
13	5.3E+05	-57.23	2.7E+05	-54.24
14	9.5E+03	-39.76	4.1E+05	-56.15
15	1.8E+02	-22.53	6.8E+05	-58.34
16	1.9E+05	-52.89	3.0E+05	-54.73
17	2.6E+03	-34.18	4.7E+05	-56.71
18	5.6E+01	-17.46	8.4E+05	-59.26

The effect of each process parameter on the S/N Ratio at different levels can be separated out because the experimental design is orthogonal. The S/N ratio for each level of the process parameters is summarized in Table 6. In addition, the total mean of the S/N ratio for the eighteen experiments is also calculated and listed in Table 6. Fig. 3 shows the S/N Ratio (Smaller-the-best) graph where the dashed line is the value of the total mean of the S/N ratio. Basically, the larger the S/N ratio, the quality characteristics for the sheet resistance and junction depth are better [11, 15].

Table 6: S/N response for the Sheet Resistance

Symbol	Process Parameter	S/N Ratio (Smaller-the-Best)			Max - Min
		Level 1	Level 2	Level 3	
A	Material	-51.66	-41.47	-	10.19
B	Time	-52.19	-45.50	-42.01	10.18
C	Temperature	-60.78	-45.96	-32.95	27.83

Overall Mean = -46.57dB

Table 7: S/N response for the Junction Depth

Symbol	Process Parameter	S/N Ratio (Smaller-the-Best)			Max - Min
		Level 1	Level 2	Level 3	
A	Material	-38.16	-56.11	-	17.95
B	Time	-45.44	-47.41	-48.55	3.11
C	Temperature	-42.89	-47.12	-51.39	8.5

Overall Mean = -47.14dB

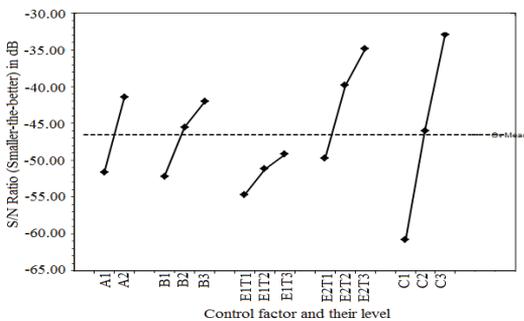


Figure 3: The S/N Ratio and mean graph for Rs

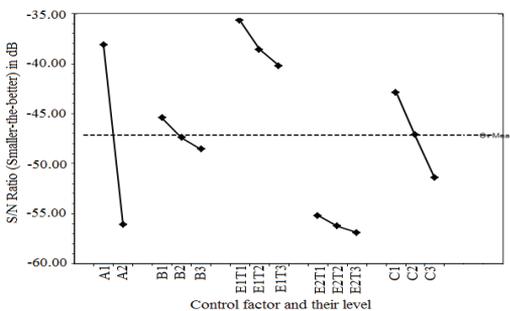


Figure 4: The S/N Ratio and mean graph for Xj

B. Analysis of Variance (ANOVA)

The effect of the different process parameter on the Rs and Xj were obtained by decomposition of variance, which is called analysis of variance (ANOVA) [4]. According to Table 8, temperature was found to be the major factor affecting the Rs (69%), whereas material (boron) was the major factor affecting the Xj (82%). Percent factor effect on S/N Ratio indicates the relative power of a factor to reduce variation. For a factor with a high percent contribution, will

have a great influence on the performance [9, 11]. In this research, material and temperature were found to be the second-ranking factor affecting the Rs (14%) and Xj (12%) respectively.

Table 8: Result of ANOVA for Rs and Xj in Shallow PN junction Device

Response	Symbol	Process Parameter	Degree of Freedom	Sum of Square	Mean square	F-Value	Factor Effect on S/N Ratio (%)
Rs	A	Material	1	468	468	26	^a 14
	B	Time	2	321	161	9	^a 10
	C	Temperature	2	2327	1164	20	^a 69
Xj	A	Material	1	1451	1451	247	^a 82
	B	Time	2	30	15	3	2
	C	Temperature	2	217	109	18	^a 12

At least 95% confidence.

In order to get the best setting that satisfies sheet resistance (Rs) and junction depth (Xj), some comparison of the best level input process parameters and factor effects among the output responses have to be done. Table 9 shows the comparison of the best level input process parameters and factor effects on SNR among the output responses. From Table 9, it can be observed that the best level of the input process parameters has been determined. There are two priorities that have to be considered in order to select the best level. First priority is whenever the majority of the same level setting that has been used will be determined as the best level without considering the factor effect on SNR. This is because when using the same level of input process parameters, the majorities will not contribute much change in the output responses. Second priority is whenever all the output responses are at the different level. The output response which has the highest factor effect on SNR will be selected as the best level.

Table 9: Comparison of the Best Level Parameters and the Factor Effects on SNR

Process Parameter Symbol	Rs		Xj		Overall Best Level
	Level	Factor Effect % on SNR	Level	Factor Effect % on SNR	
A	2	14	1	82	1
B	3	10	1	2	3
C	3	69	1	12	3

Factor A has the different level on each output response but level 1 of factor A has the highest factor effect on SNR for Xj. Therefore, level 1 of factor A is selected as the best level. Factors B and C also have the different level on each output response, but level 3 of both factors have the highest factor effect on SNR for Rs and Xj. Therefore, level 3 of factors B and C are selected as the best level. Therefore, the best level setting of process parameters was selected as A₁, B₃ and C₃.

C. Confirmation Test

The confirmation test is used to verify the estimated result with the experimental results. Best setting of the process parameters for Shallow PN junction device that has effects on the output response which was suggested by Taguchi Method is shown in Table 10.

Table 10: Best Setting of the Process Parameters for Xj and Rs

Symbol	Process Parameter	Unit	Level	Best Value
A	Material	-	1	boron
B	Time	minutes	3	45
C	Temperature	°C	3	950

The confirmation test is not required in Shallow PN junction device design because the optimum combination of parameters and their levels, i.e. A₁, B₃ and C₃ respectively do correspond to experiment 9 of the orthogonal array (refer to Table 2). In the optimization approaches, the S/N ratios (smaller-the-best) of Rs and Xj for shallow PN junction device are -39.45dB and -46.77 dB respectively as shown in Table 11. Both values are within the predicted range. Figure 4.8 shows a graf results from the confirmation experiment for Xj and Rs.

Table 11: Results of the confirmation experiment for Xj and Rs

Output Response	Set 1 (U1V1)	Set 2 (U1V2)	Set 3 (U2V1)	Set 4 (U2V2)	SNR (Smaller-the-best)
Rs (Ω/cm ²)	93.865	93.923	93.78	93.829	-39.45
Xj (nm)	218.07	218.01	218.16	218.11	-46.77

For Rs, -39.45dB is within the predicted range S/N ratio of -26.97dB to -40.01dB (-33.49±6.52dB). While for Xj, -46.77dB is within the predicted range S/N ratio of -40.16dB to -47.50dB (-43.83±3.67dB).r

The graph result of the confirmation experiment for Xj and Rs.

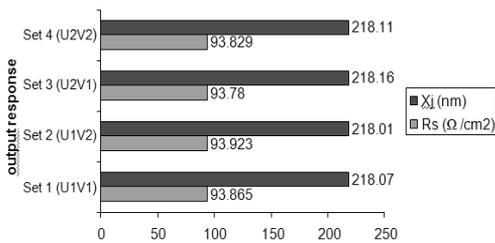


Figure 5: Confirmation experiment for Xj and Rs

These indicate that Taguchi method can predict the optimum solution in finding the Shallow PN junction fabrication recipe with small Xj and Rs values. The result shows that material (boron) and temperature have the strongest effect on Xj and Rs respectively. P-N Junction device has anode and cathode

terminals. Junction depth (Xj) was colored yellow layer. This output structure was found when the simulation fabrication of the shallow P-N junction device runs. The material for N type is boron, and the material for P type is phosphorus.

This design method gave eighteen set experiments. The analysis of variance shows the process parameter of material (boron), and temperature are significant based on 95% confidence level towards junction depth and sheet resistance respond in the shallow PN junction device [12]. So that the junction depth and sheet resistance decreased follows the material (boron) and temperature.

IV. CONCLUSION

This design method gave 18 set experiments. It has many variants that can be applied to the modeling device, and a lot of parameters can be used. The analysis of variance shows the process parameter of temperature, and material (boron) are significant based on 95% confidence level towards sheet resistance and junction depth respectively respond in the shallow PN junction device. So that the sheet resistance and junction depth decreased follows the temperature and material (boron) respectively. Analysis of variance also proved the factors of temperature, and material are significant for both response, sheet resistance and junction depth.

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REFERENCES

- [1] Polo Gargini. The International Technology for Semiconductors (ITRS): 'Past, present and Future'. 22nd Annual Gallium Arsenide Integrated Circuit (GaAs IC) Symposium: IEEE pp 3-5, (2000).
- [2] N. Osman and R.sanudin. Gate length effect on NMOS Electrical Characteristic Using TCAD Tools. Engineering Postgraduate Conference: EPC, (2008)
- [3] Toan, N. N., (1999), *Spin on Glass Materials and Applications in Advanced IC Technologies*. PhD Thesis: University of Twente.
- [4] U.Hashim. Shallow Junction Formation: A Simulation baSED Study of Thermal Diffusion By Spin-on-dopands Technique. *Journal of Applied Sciences Reseach*, vol(8), PP.1154-1161,2012.
- [6] Nik hazura N.Hamat, uda Hashim, Ibrahim Ahmad, (2006), *Simulation of Ultra Shallow Junction Formation for Nano Devices Application by Dopant Diffusion from Spin on Glasses*, Jurnal Teknologi Universiti Teknologi Malaysia, 45(D), pp. 153-165.
- [7] Fauziyah Binti Salehuddin, (2003), *Simulasi bagi pembentukan simpangan cetek menggunakan resapan dopan daripada SOD (Spin On Dopant)*, Master Thesis: Universiti Kebangsaan Malaysia, Bangi, Selangor.
- [8] Robust Engineering, Genichi Taguchi, Subir Chowdhury, and Shin Taguchi, (2000), McGraw Hill, New York
- [9] Taguchi Methods, Glen Stuart Peace, Addison Wesley (1993)
- [10] Bala Murugan Gopalsamy, Biswanath Mondal and Sukamal Ghosh, "Taguchi method and ANOVA: An approach for process parameters optimization of hard machining while machining hardened steel".*Journal of Scientific and Industrial Research*, Vol. 8, August (2009) pp. 686-695

- [11] F. Salehuddin, I. Ahmad, F.A. Hamid, A. Zaharim, U. Hashim, and P.R. Apte, "Optimization of Input Process Parameters Variation on Threshold Voltage in 45nm NMOS Device", *International Journal of the Physical Sciences*, Vol.6(30), pp.7026 – 7024, 2011.
- [12] Hong-Sik Shin, Se-Kyung Oh, Min-Ho Kang, In-Shik Han, Hyuk-Min Kwon, Sang-Uk Park, Byung-Seok Park, Jung-Deuk Bok, Ga-Won Lee, and Hi Deok Lee. Improvement Of Junction Characteristics of Ultra Shallow Junction With Boron - Cluster Implantation and Ni-Silicide For Nano-scale CMOS technology, 2009.
- [13] Tijjani Adam and Uda Hashim. Low Resistance Electrical Layer Formation: A Simulation Study of Diffusive Rapid Thermal Process on Implanted Dopant Species for Electronic Actives Devices. Fourth International International Conference on Computational Intelligence, Modeling and Simulation. 2012.
- [14] Kil-Ho Lee. Effect of Additional Low Temperature RTA on ultra – shallow p+-n Junction Formation. IEE Journal, 1997, 634.
- [15] H.A. Elgomati, B.Y. Majlis, I. Ahmad, F. Salehuddin, F.A. Hamid, A. Zaharim, and P.R. Apte, "Application of Taguchi Method in the Optimization of Process Variation for 32nm CMOS Technology", *Australian Journal of Basic and Applied Sciences*, Vol.5(7), pp.346–355, 2011.