

## ETCHING PERFORMANCE IMPROVEMENT ON SEMICONDUCTOR SILICON WAFERS WITH REDESIGNED ETCHING DRUM

ROZZETA DOLAH<sup>1</sup>, HAMIDON MUSA<sup>2</sup> & ASTUTY AMRIN<sup>3</sup>

**Abstract.** Etching process involves various chemical reactions and reflects significantly on the silicon wafer quality. The paper addresses the major problem on wafers during etching that is wafer removal distribution throughout etching drum compartment. The etchant used in this study were the composition of HNO<sub>3</sub>, HF, and CH<sub>3</sub>COOH. The etching drum has been redesigned to overcome the lower removal problem at the end of each compartment and to reduce the big disparity in wafer removal distribution. The proposed idea is to install a piece of “circumferential acid resistant PVC wafer” for the remaining empty slot (empty area without wafers) at each end of a compartment. The permanent PVC piece with certain gap at each end is then fabricated for the new drum design. The characteristics of the end wafers are compared with other wafers in the compartment to study the etching difference that leads to this problem. Surface morphology and surface roughness parameters (arithmetic roughness mean; Ra and surface skewness [roughness root mean square]; Rms) using atomic force microscopy (AFM) comparison between old drum design (big wafer gap) and new drum design (smaller gap with additional PVC chip) had been analyzed. The uniformity without lower removal problem at the end compartment is observed in removal distribution graph.

**Keywords:** Etching process; surface micromachining; silicon wafer; etching removal; silicon wafer surface roughness

**Abstrak.** Proses *etching* atau punaran melibatkan pelbagai tindak balas kimia dan sangat penting dalam menentukan kualiti wafer silikon. Projek ini menyelesaikan masalah utama wafer ketika proses punaran, iaitu keserakan data pembuangan sisa wafer di sepanjang dram punaran. Cecair punaran yang digunakan dalam projek ini terdiri daripada komposisi asid HNO<sub>3</sub>, HF, and CH<sub>3</sub>COOH. Dram punaran telah diubahsuai untuk menyelesaikan masalah pembuangan sisa wafer yang rendah di setiap wafer pertama dan terakhir dalam sesuatu kompartmen dram. Tujuan utamanya adalah untuk mengurangkan jurang perbezaan variasi dalam pembuangan sisa wafer, di mana nilai pembuangan silikon adalah rendah berbanding pembuangan silikon wafer di tengah kompartmen. Antara cadangan tersebut adalah menambahkan “kepingan wafer PVC tahan asid”

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<sup>1,3</sup> RAZAK School of Engineering and Advanced Technology, Universiti Teknologi Malaysia, 54100 Kuala Lumpur

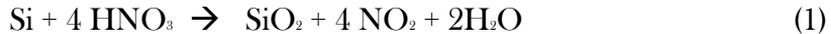
<sup>2</sup> Department of Manufacturing, University Teknologi Malaysia, 81310 UTM Johor Bahru

di sebelah wafer pertama dan terakhir dalam setiap kompartmen. Selepas memperoleh keputusan yang memberangsangkan, kepingan PVC tersebut dikekalkan dalam rekabentuk dram yang baru. Sifat wafer pertama dan terakhir dinilai untuk memastikan tiada kualiti yang terjejas berbanding wafer-wafer di tengah kompartmen. Morfologi permukaan dan kekasaran wafer (purata kekasaran;Ra dan kekasaran “skewness”;Rms) menggunakan mikroskop tujahan atom (AFM) dianalisis untuk dibandingkan dengan dram lama. Keseragaman pembuangan wafer tanpa masalah pembuangan rendah di hujung kompartmen telah diperhatikan

*Kata kunci:* Proses punaran, permukaan “Micromachining”, wafer silicon, pembuangan silicon wafer, kekasaran permukaan wafer silikon

## 1.0 INTRODUCTION

In silicon wafer manufacturing, the most commonly used etchant used is  $\text{HNO}_3$  - HF, with etchant modifiers such as acetic acid,  $\text{CH}_3\text{COOH}$ , are used. Etchant composition for wafer fabrication normally consists of  $\text{HNO}_3$ :HF: $\text{CH}_3\text{COOH}$  = 39.3%:11.6%:20.9%. Chemical etching with this etchant system proceeds with the following two step reaction:

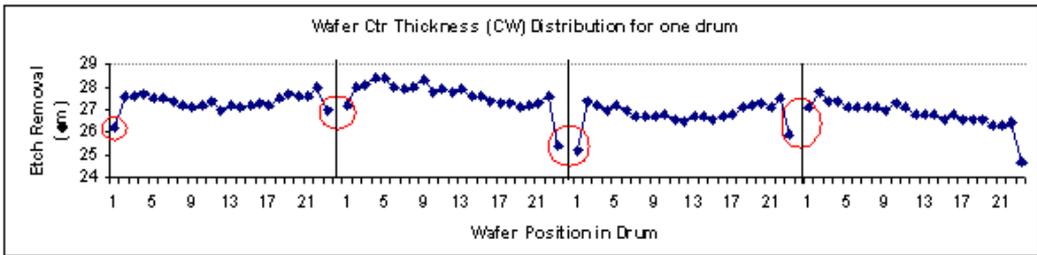


and



The etching reactions are exothermic [4] and the temperature control is critical for uniform etching. The reaction product  $\text{NO}_x$  is toxic, and safety controls must be used. The silicon wafer is dipped into the chemical etchant to remove entirely the mechanical damage induced by previous processes, such as lapping. After etching, the wafer should be bright and the removal values within specifications. Etching parameters are set on control panel at the acid etching machine. The main output parameters of etching studied here is the etching removal.

Currently, variations in wafer thickness removed during etching are observed within a compartment especially with wafers positioned at the two ends of each of the four compartments. Figure 1 depicts a typical profile of etching thickness removed (labeled as etch removal) for a batch of wafers in one etching drum, which has four compartments. The reduced etch thickness removed from eight wafers on each side of the four drum compartments are indicated by the eight low spikes.



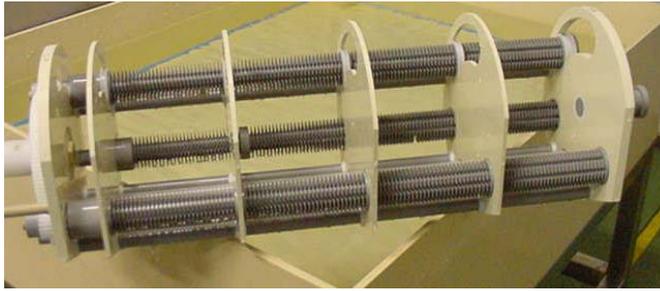
**Figure 1** Low spike at beginning and end of each compartment

\*NB: Etching removal = wafer thickness before etching (lapped thickness) MINUS wafer thickness after etching

It is thought that the above variations are due to various etching and etchant parameters, such as uniformity of etchant flow rate (referred to as bubbling flow rate), variation in acid temperature, silicon content in the etchant, etching drum groove dimension, existence of gaps between compartments in the etching drum and so on [11][3]. In order to fully address this challenge, many aspects need to be investigated. An improved drum design will be developed, and it is made as a basis for further and more comprehensive investigation.

## 2.0 EXPERIMENTAL AND METHODOLOGY

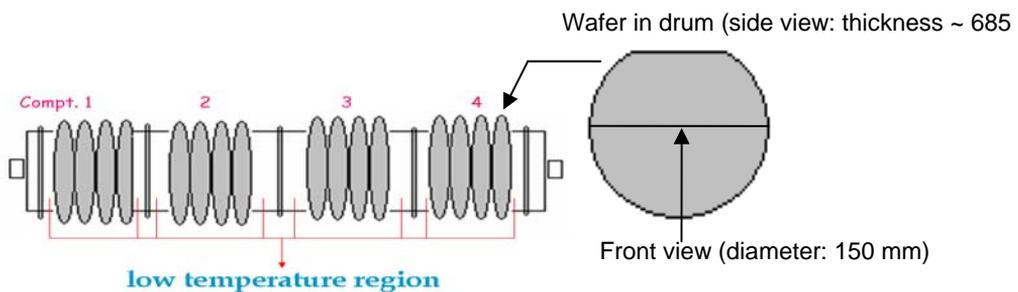
The etching process done here is an isotropic etching type, in which etching happens in all directions [25]. Wafers are loaded inside a basket, which contains 23 pieces of wafer. The etching arrangement employs one etching drum that can accommodate up to four baskets, with one basket fitting into one compartment. Thus, one etching drum contains of four compartments. This means that at any time, 92 pieces of wafer can be etched (23 pieces  $\times$  4). Figure 2 below shows the old etching drum:



**Figure 2** The old etching drum

It is possible that removal variations are due to non-uniform etchant flow rate. The etching drum is composed of the compartment divider, horizontal rollers, each having circumferential grooves cut in the surface. The wafers are closely spaced about 4 to 7 mm apart. During etching, the drum will rotate at certain rotation, approximately 25 to 40 rpm and wafers tend to produce liquid rotation and turbulence. Consequently, it has led to non uniform etching across individual wafers and along the compartment. Having said that, wafers located at each end of a compartment suffer the most unstable removal.

In etching compartment (compt.), there are 29 slots per compartment. 23 wafers will be positioned in each compartment, using slot numbers 3 to 26. Slot numbers 1, 2, 27, 28, and 29 will be left empty. It is suggested that this gap means that a cooler region may exist next to the nearest wafers resulting in significant lower removal of these wafers (refer to Figure 3):



**Figure 3** Low temperature region

A new drum is designed in a way to ensure a comparable turbulence to all wafers in a drum. The end gap is minimized by adding a PVC plate at each side of a compartment as shown in Figure 4.

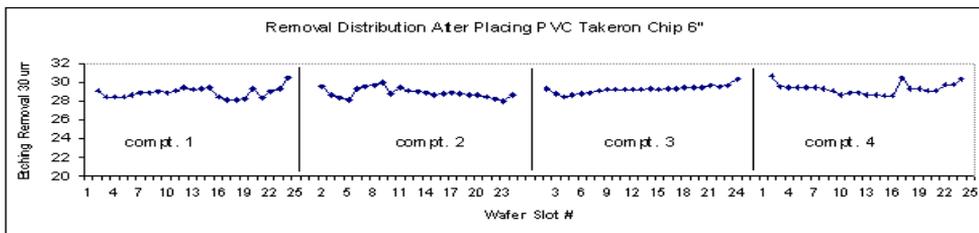


**Figure 4** New etching drum

### 3.0 EXPERIMENTAL RESULTS

#### 3.1 Etching Removal Result

The redesigned drum is fabricated. Consequently, as in Figure 5, lower spike at end of each compartment is minimized. This has improved the removal distribution throughout the drum. With the new drum design, it the temperature in the area has been balanced with the remaining area of the compartment and they ensure that end wafers have sufficient removal. This phenomenon is supported by MEMC patent [15]. When wafers are closely spaced, rotations of wafers tend to produce a rigid body rotation of the liquid between the wafers. By adding PVC casing in etching drum, it improves the uniformity of etching.



**Figure 5** Removal distribution after using the new drum

End compartment lower peak has improved. In the data summary, we aim for the smallest range of etching removal, smallest standard deviation (STDEV), and smallest Total Thickness Variation (TTV). Data summary is shown below:

(i) Figure 6:

XKSL 501

No	Drum test	Ingot No.	Range (etch removal) um			Etching Removal: um		DELTA TTV		DELTA STIR	
			Max	Min	delta	STDEV	AVG	STDEV	AVG	STDEV	AVG
1	NEW	XKSL 501 - 37854	37,9	33,8	4,1	1,239	35,6	0,639	0,8	0,889	0,70
2	OLD	XKSL 501 - 37735	41,0	28,2	12,8	2,095	35,9	0,283	0,8	0,144	0,50

Hence, more data is collected using the new drum:

(ii) Figure 7:

XKSS 500

No	Drum test	Ingot No.	Range (removal)			Center Thickness		DELTA TTV		DELTA STIR	
			Max	Min	delta	STDEV	AVG	STDEV	AVG	STDEV	AVG
1	NEW	XKSS 500 - 37854	38,7	32,0	4,7	1,286	34,5	0,478	0,5	0,386	0,50

(iii) Figure 8:

XTUM 527

No	Drum test	Ingot No.	Range (removal)			Center Thickness		DELTA TTV		DELTA STIR	
			Max	Min	delta	STDEV	AVG	STDEV	AVG	STDEV	AVG
1	NEW	XTUM 527	36,4	31,4	5,0	1,35	34,01	0,565	0,664	0,395	0,48

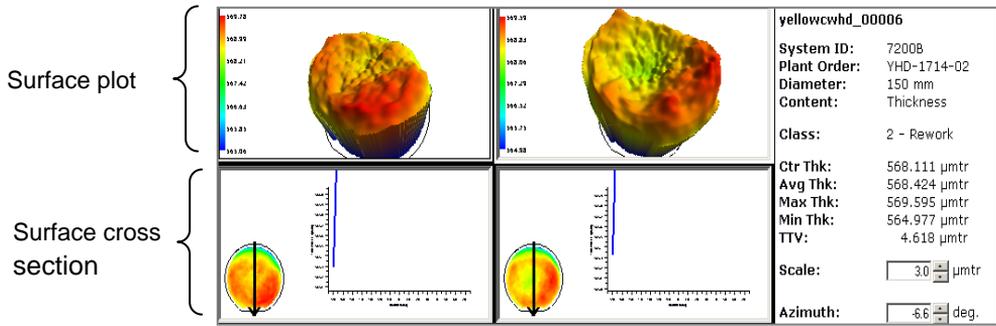
(iv) Figure 9:

WKSS 702 - 10315

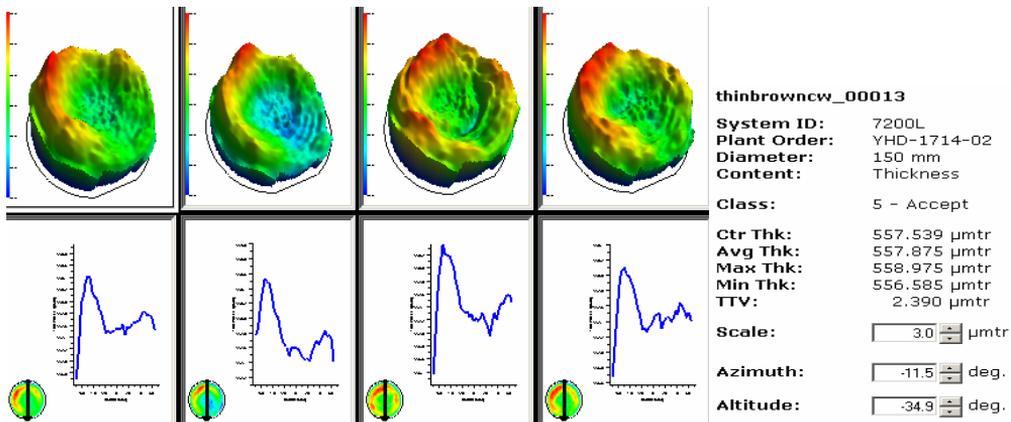
No	Drum test	Ingot No.	Range (removal)			Center Thickness		DELTA TTV		DELTA STIR	
			Max	Min	delta	STDEV	AVG	STDEV	AVG	STDEV	AVG
1	NEW	WKSS 702	39,0	33,2	5,8	1,244	36,67	0,272	0,9	0,167	0,60

### 3.2 Surface Morphology

Surface after etching is captured by the ADE software. The purpose of this analysis is to compare the etching removal surface for gap wafers and near wafers. It shows that gap wafers seem to have lack of removal, resulting in thicker wafers. The results are as in Figure 10:



**Figure 10** End wafer surface profile (with gap)

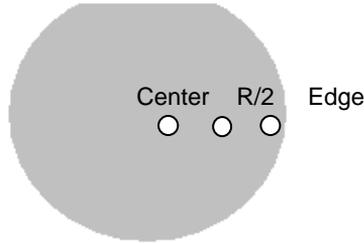


**Figure 11** Middle wafer surface profile (No gap, wafer is close to each other)

Middle wafer has sufficient removal and desired concave shape as shown in Figure 11. From the results above, it is clear that PVC chips help to eliminate the lower peak at every end of each compartment. It is thought that the lower removal is caused by imbalanced turbulence due to the wider drum slot at the end side of a compartment. The chips placed in wider slot seem to have overcome the problem to ensure a balance spread of etchant, similar to that in between the wafers.

In addition, silicon wafer surface morphology is studied on its roughness to observe the wafer appearance under this two conditions; with gap (no pvc chip) and no gap (with pvc chip). The instrument used for wafer surface analysis is Atomic Force Microscopy (AFM). Figure 12 shows the AFM measured point on

wafer surface and its arithmetic mean roughness (Ra) and surface skewness (Rms) result.



WAFER	LOCATION	Ra (Roughness mean in nm)	Rms (Roughness root mean square in nm)
OLD DESIGN (no PVC chip) - sample 1	Center	112.58	146.67
	R/2	135.28	172.99
	Edge	126.23	169.44
OLD DESIGN (no PVC chip) - sample 2	Center	77.146	97.835
	R/2	80.582	100.42
	Edge	146.46	187.46
NEW DESIGN (with PVC chip) - sample 1	Center	77.908	101.07
	R/2	63.865	84.487
	Edge	68.428	86.633
NEW DESIGN (with PVC chip) - sample 2	Center	59.518	76.459
	R/2	64.008	84.403
	Edge	61.909	79.598

**Figure 12** AFM measured points and roughness results

From the result above, drum with PVC chips give lower surface roughness, compared to wider gap wafer (without chips). Rms average value for near gap is much lower that is 85.44 compared to 145.79 for wider gap.

ANOVA Table for Rms by TYPE

Analysis of Variance					
Source	Sum of Squares	Df	Mean Square	F-Ratio	P-Value
Between groups	10930.3	1	10930.3	14.09	0.0038
Within groups	7756.93	10	775.693		
Total (Corr.)	18687.2	11			

ANOVA Table for Ra by TYPE

Analysis of Variance					
Source	Sum of Squares	Df	Mean Square	F-Ratio	P-Value
Between groups	6657.21	1	6657.21	15.33	0.0029
Within groups	4342.55	10	434.255		
Total (Corr.)	10999.8	11			

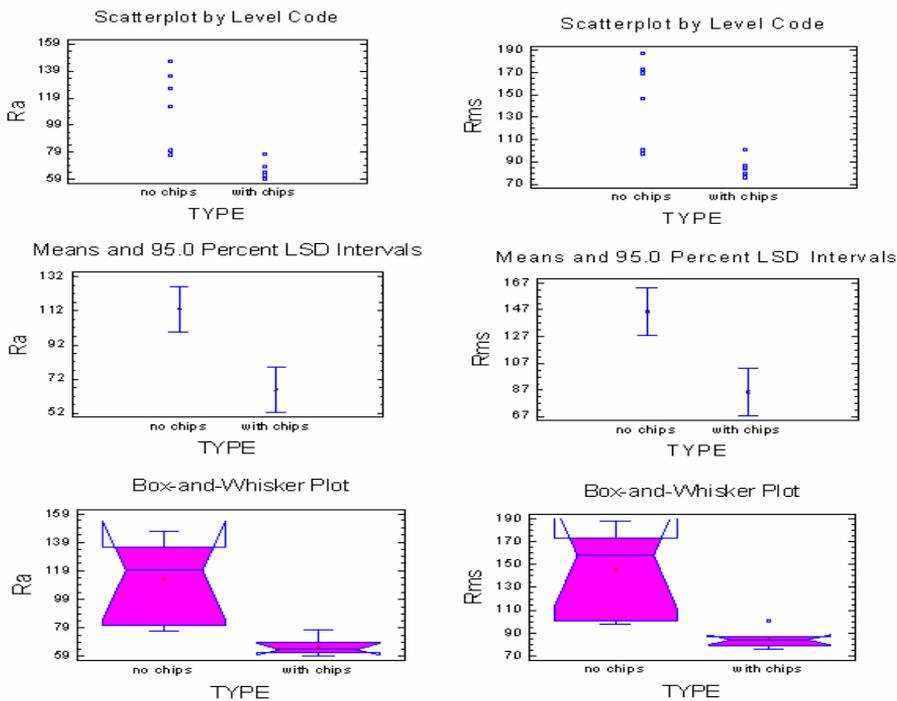


Figure 13 Statistical analysis on surface roughness

Surface roughness from AFM analysis in Figure 14 shows that without PVC chips wafers have rougher surface compared with PVC chips which provide smoother surface:

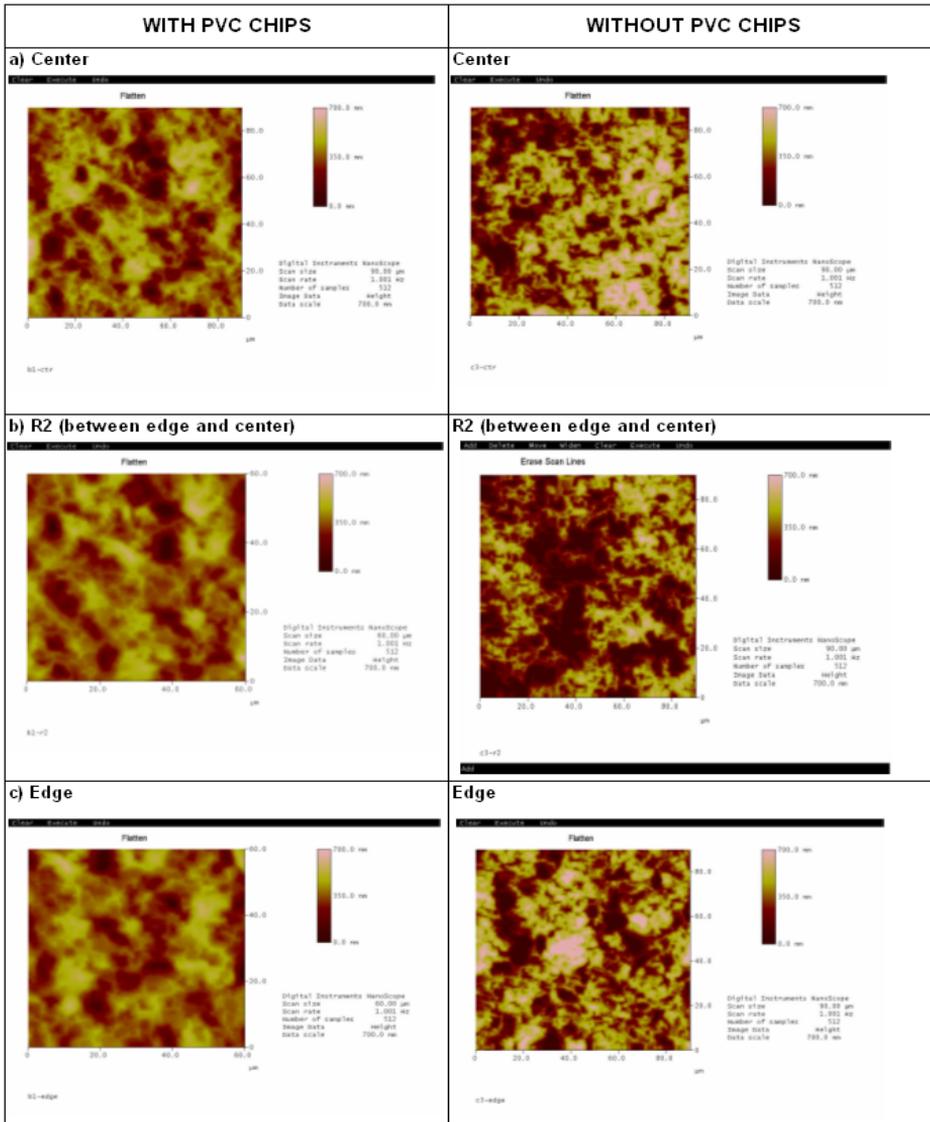


Figure 14 AFM surface morphology

## 4.0 CONCLUSION

Basically, the new drum has a better performance than the old ones. In initial experiments, the new drum has helped rectify the low spike at each end of a compartment. Low spike that is due to lower removal is caused by the cooler temperature region. Consequently, the cooler region leads to lower temperature area. Etchant with lower temperature does not have reactive etching activity. Thus, the surface is not being etched properly and will result in less etching removal. Wafer tends to be rejected as thick wafers and did not meet the thickness specification. On the other hand, higher etchant temperature serves active etching reaction and result in higher removal. Etching surface profile and surface roughness between gap and near wafers are studied to understand the consequences behind non-uniformity removal.

The new drum performance has been further studied with other etching parameters to target for a more uniform etching removal within wafers throughout all four compartments. The result clearly indicates that compartments 1 and 4 have slightly lower removal compared to compartments 2 and 3. The etched surface would not have the same surface profile although the etching removal is quite comparable to each other. These tests have shown that the production of foamed concrete with predictable densities and strengths is only possible with protein foam. This investigation was therefore conducted using only this type of foaming agent. All the materials used were produced in Malaysia, and only one source of protein agent, cement, and superplasticizer was used.

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## REFERENCES

- [1] A. Gordijn, J. K. Rath, R. E. I. Schropp. 2004. Microcrystalline Silicon Growth in the Presence of Dopants: Effect on High Growth Temperatures. *Journal of Non Crystalline Solids*. 338-340:110-114.
- [2] Dana Cristea, *et al.* 2002. Experiments for Microphotonic Components Fabrication using Si <111> Etching Techniques. *Sensors and Actuators*. 99: 92- 97.
- [3] D. J. Blackwood, Y. Zhang. 2003. The Effect of Etching Temperature on the Photoluminescenes Emitted from, and the Morphology of P-type Porous Silicon. *Journal of Electrochemical*. 48: 623-630.
- [4] E.Chambon, E. Florentin *et al.* 2005. Optical Properties of Porous Silicon Surface. *Microelectronics Journal*. 36: 514-517.
- [5] E. Vazsonyi, E. Szilagyi, P. Petrik, Z. E.Horvath, T. Lohner, M. Fried, G. Jalsovzky. 2001. Porous Silicon Formation by Stain Etching. *Thin Solid Film*. 388: 295- 302.
- [6] H. Bidadi, S.Sobhanian, M. Mazidi, S. H. Hasanli, S. Khorram. 2003. The Peculiarities of Mechanical Bending of Silicon Wafers after Diverse Manufacturign Operations. *Microelectronics Journal*. 34: 515-519.
- [7] J. Watanabe, G. Yu, *et al.* 2005. High Precision Chemical Mechanical Polishing of Highly Boron-doped Silicon Wafer used for Epitaxial Substrate. *Precision Engineering*. 29:151- 156.
- [8] J. Tan, S. X Lee, Y. Wan, F. Li, K. Lu. 2003. Crystallographic Cracking Behavior in Single Crystal Wafer. *Journal of Material Science and Engineering*. B103: 49-56.
- [9] Kalpakjian, R. Schmid. 2001. *Manufacturing Engineering and Technology*. 4<sup>th</sup> ed. New Jersey: Prentice Hall International.
- [10] Kuide ,Q. Yongcheng, L. 2003. Mechanisms of Particle Removal from Silicon Wafer Surface in Wet Chemical Cleaning Process. *Journal of Colloid and Interface Science*. 261: 569- 574.
- [11] Kuo, S. C., Xin, Z., Arturo, A. A., S. Mark Spearing. 2002. Effect of Process Parameters on the Surface Morphology and Mechanical Performance of Silicon Structures after Deep Reactive Ion Etching (DRIE). *Journal of Microelectromechanical Systems*. 11: 3.
- [12] Lunsford, C. 1992. *The St. Martin's Handbook*. New York: St. Martin's Press.
- [13] Lun, B. X. 1998. The Formation of an Inhomogeneous Distribution of Oxygen in CZ-Silicon Crystal: An Investigation with Quantum Reaction-Diffusion Equation. *Journal of Crystal Growth*. 193: 541-551.
- [14] M. Barranco Diaz, W. Koch *et al.* 2002. Resistivity Topography: A Grain Boundary Characterization Method. *Solar Energy Materials and Solar Cells*. 72: 473- 486.
- [15] MEMC Electronic Materials, Inc., International Publication no.: WO 95/10850. 20.04.1995.
- [16] M. Safi, J. N. Chazalviel, M. Cerkaoui, A. Belaidi, O. Gorochov .2002. Etching of n- type Silicon in (HF + oxidant) Solutions: in situ Characterization of Surface Chemistry. *Journal of Electrochemical*. 47: 2573- 2581.
- [17] M. Vergnat, N. Hadj Zoubir, A.Burneau. 1995. Homogeneous Chemical Etching of Sandblasted Silicon Substrates. *Thin Solid Films*, 255: 231- 233.
- [18] Mei Sun, Kevin Gabriel. Direct Wafer Temperature Measurement for Etch Chamber Diagnostics and Process Control. USA.
- [19] N.Gabouze. 2002. A New Preferential Etch of Silicon (111) with Ammonia System. *Surface Science*. 507-510: 429-433.
- [20] P. K. Singh, R. Kumar, M. Lal, S. N. Singh, B. K. Das. 2001. Effectiveness of Anisotropic Etching of Silicon in Alkaline solutions. *Solar Energy Materials and Solar Cells*. 70: 103- 113.

- [21] S. Beyer, S. Lohr, Ch. Heyn, D. Heitmann, W. Hansen 2002. Etching Temperature Dependant Mobilities up to  $190 \text{ cm}^2/\text{Vs}$  at Chlorine Etched and Regrown Interfaces. *Journal of Physics*. 653-656.
- [22] Seth P. Bates. 2000. Silicon Wafer Processing. Applied Materials, Summer.
- [23] Sharath Chandrasekaran, Sriram Sundararajan 2004. Effect of Micofabrication Processes on Surface Roughness Parameters of Silicon Surfaces. *Surface and Coating Technology*. 188- 189: 581- 587.
- [24] Shimura, F. 1989. *Semiconductor Silicon Crystal Technology*. Academic Press, Inc. San Diego, California.
- [25] T. H.Wetzel, J.Virbulis. 2003. Modelling in Industrial Silicon Wafer Manufacturing - From Crystal Growth to Device Processes. *International Scientific Colloquium*, Modeling for Electromagnetic Processing, Hannover. March 24- 26.
- [26] Wataru Natsu, Yukihiro Ito *et al.* 2005. Effects of Support Method and Mechanical Property of 300 mm Silicon Wafer on Sori Measurement. *Precision Engineering*. 29: 19-26.
- [27] X. P. Li, T. He, M. Rahman. 2005. Tool Wear Characteristics and Their Effects on Nanoscale Ductile Mode Cutting of Silicon Wafer. *Wear*. 259:1207- 1214.
- [28] Yanbing Zu, Lie Xie *et al.* 1998. Studies on Silicon Etching using the Confined Etchant Layer Technique. *Journal of Electrochemical*. 43: 1683- 1690.