

GATE DEPLETION ANALYSIS OF PMOSFETS WITH POLYSILICON GATE

Norhayati Soin and Desmond Soo Chin Yoong

Electrical Department, Faculty of Engineering, University of Malaya

ABSTRACT

This paper presents the study of the polysilicon gate depletion effect (PDE) on the threshold voltage and capacitance of PMOSFETs devices. Simulation analysis over wide range of oxide thickness, gate length width and gate doping were also performed. Simulation results proved that the polysilicon gate depletion effect caused the performance degradation in MOSFET devices due to the reduction of the total gate capacitance as the potential drop of the gate increased. The PDE effect of PMOSFETs with silicon nitride (Si_3N_4) as dielectric material has been proved to have better performance than the PMOSFETs with silicon dioxide (SiO_2) dielectric. It has been found that the polysilicon gate is not compatible to High-K dielectric material.

INTRODUCTION

Polysilicon gate depletion is an effect that degrades the circuit performance of deep submicron standard CMOS technologies. It is undesired effect caused by interaction with High-K gate dielectric in the MOS stack [1]. Polysilicon depletion effects significantly degrade the capacitance of the MOSFET devices. For a small device, polysilicon depletion effects can no longer be ignored. These effects are directly related to the high electric fields [2]. Polysilicon depletion effect (PDE) occurs due to the insufficient doping and insufficient activation dopant near the polysilicon- SiO_2 interface that eventually caused the performance of the MOSFET to degrade [2]. The objective of this paper is to investigate the gate depletion effect on PMOSFETs devices with different types of dielectric material.

DEVICES AND SIMULATION CONDITIONS

The simulation study has been performed by using device simulation software, MINIMOS 6.1 [4]. Several p-channel MOSFETs with different type of dielectric materials were simulated for different channel lengths and oxide thicknesses. All simulated devices have been modeled with p-type polysilicon, gap distance between the polysilicon gate and source or drain of $0.5\mu\text{m}$, polysilicon thickness of $0.2\mu\text{m}$, substrate doping concentration of $1 \times 10^{17}\text{cm}^{-3}$. For source/drain doping, boron dopant has been used. Given also the implant dose, implanted energy and annealing condition (i.e., time and temperature), MINIMOS can yield the doping profile in the polysilicon gate.

POLYSILICON DEPLETION MODELING

For an n+ polysilicon NMOSFET or p+ polysilicon PMOSFET, the relationship between the gate bias V_{gs} , the voltage drop on the polysilicon gate due to the polysilicon depletion effect, V_{poly} , the voltage drop across the gate oxide, V_{ox} , the flatband voltage, V_{fb} , N_{poly} , the gate doping and substrate surface potential, $\Psi_s - 2\Phi_B$, can be written as follows [3]:

$$V_{gs} - V_{fb} = \Psi_s = V_{poly} + V_{ox} \quad (1)$$

Substitute this equation into the following equation for V_{poly} [4],

$$V_{poly} = \epsilon_{ox}^2 E_{ox}^2 / 2q\epsilon_s N_{poly} \quad (2)$$

The effective gate voltage can be applied to MOSFETs, $V_{gs_{eff}}$, can be found as follows [4]:

$$V_{gs_{eff}} = V_{fb} + 2\Phi_B + \frac{q\epsilon_s N_{poly} t_{ox}^2}{\epsilon_{ox}^2} \times \left[\sqrt{1 + \frac{2\epsilon_{ox}^2 (V_{gs} - V_{fb} - 2\Phi_B)}{q\epsilon_s N_{poly} t_{ox}^2}} - 1 \right] \quad (3)$$

Where $q = 1.6 \times 10^{19}$ C, ϵ_s and ϵ_{ox} are the relative permittivity of silicon and silicon dioxide respectively, E_{ox} is the electric field across gate oxide and t_{ox} is the gate oxide thickness. It can be noted that V_{poly} cannot exceed 1.12 V when the polysilicon itself is at strong inversion. Polysilicon depletion effect is included when V_{gs} is replaced by $V_{gs_{eff}}$ of equation 2 in MOSFET I-V equation.

RESULTS AND DISCUSSION

Effect of gate doping (P_{DOP}) on potential drop

The simulation result of the effect of the gate doping on the potential drop of pMOSFETs is shown in Figure 1. It can be seen that when the gate doping level is increased the potential drop in the gate is reduced. When the voltage drop in the gate is reduced, the voltage across the gate will be increased. For a lower level gate doping, the voltage drop will be increased [3]. When the voltage drop in the gate is increased, the gate voltage will be reduced. Therefore, when the effective gate voltage is reduced, then the voltage drop will increase in terms of magnitude. To prevent the doping in polysilicon from entering the thin oxide, implant dose with relatively low energy is preferred [5]. In addition to that, it also provides insufficient doping in the polysilicon gate close to the oxide which will eventually cause polysilicon depletion effect.

When applying a negative gate voltage, a depletion layer is formed on a polysilicon gate. Polysilicon gate depletion layer results in a voltage drop, according to [4]:

$$V_p = \frac{\epsilon_{ox}^2 E_{ox}^2}{2q\epsilon_{si}N_p} \quad (4)$$

The voltage drop in the polysilicon, V_p , reduces the effective gate voltage with the increases of the electrical thickness of the oxide.

Effect of oxide thickness (t_{ox}) on potential drop

The voltage drop in the polysilicon, V_p , reduces the effective gate voltage and increases the electrical thickness of the oxide [6-7]. The increase of the effective electrical oxide thickness will increase the potential drop in the polysilicon gate. Therefore from $C = \frac{dQ}{dV}$, V_p is proportional to t_{ox} . Therefore when the t_{ox} is increased, the potential drop will increase and the effective gate voltage will be reduced. Figure 2 shows that as the gate voltage is reduced, the potential drop is increased in terms of magnitude. As the oxide thickness is reduced, the potential drop is also reduced which leads to the increment of the gate voltage. The increase of gate voltage will reduce the potential drop in the gate in terms of magnitude. Furthermore, the polysilicon depletion effect reduces the inversion charge density and transconductance especially as the oxide thickness is scaled down to a small dimension [8].

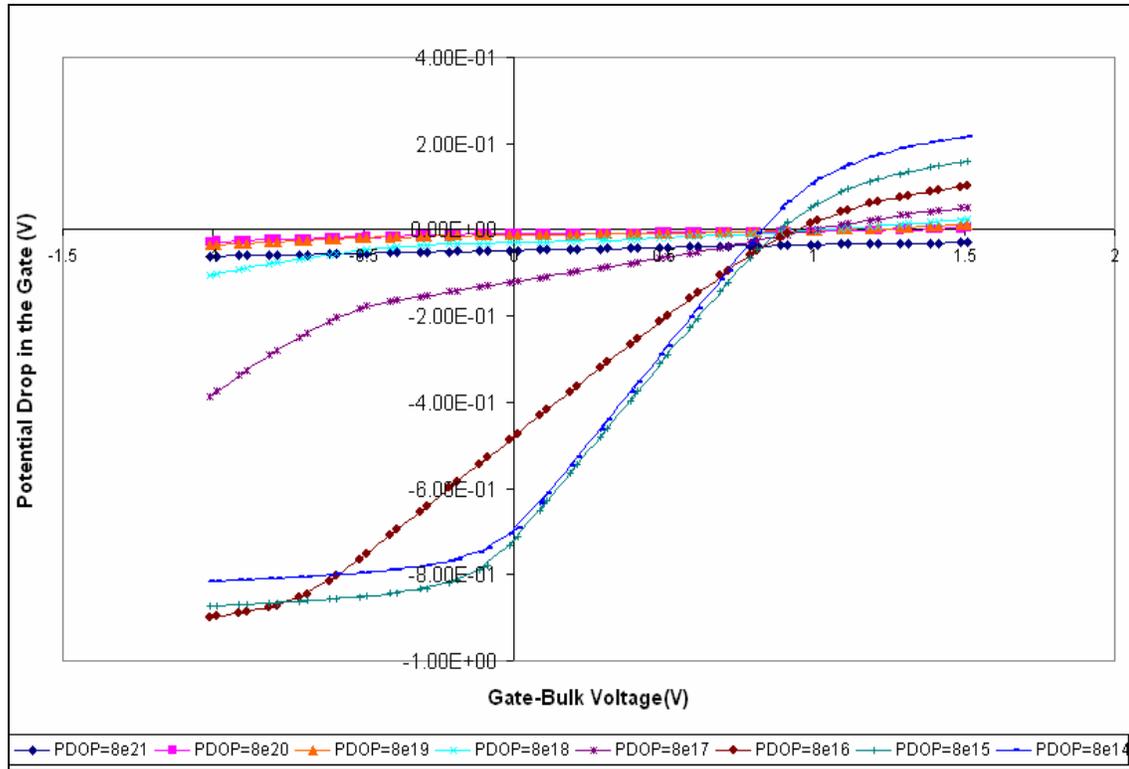


Figure 1: Potential drop vs. gate-bulk voltage for various gate doping levels

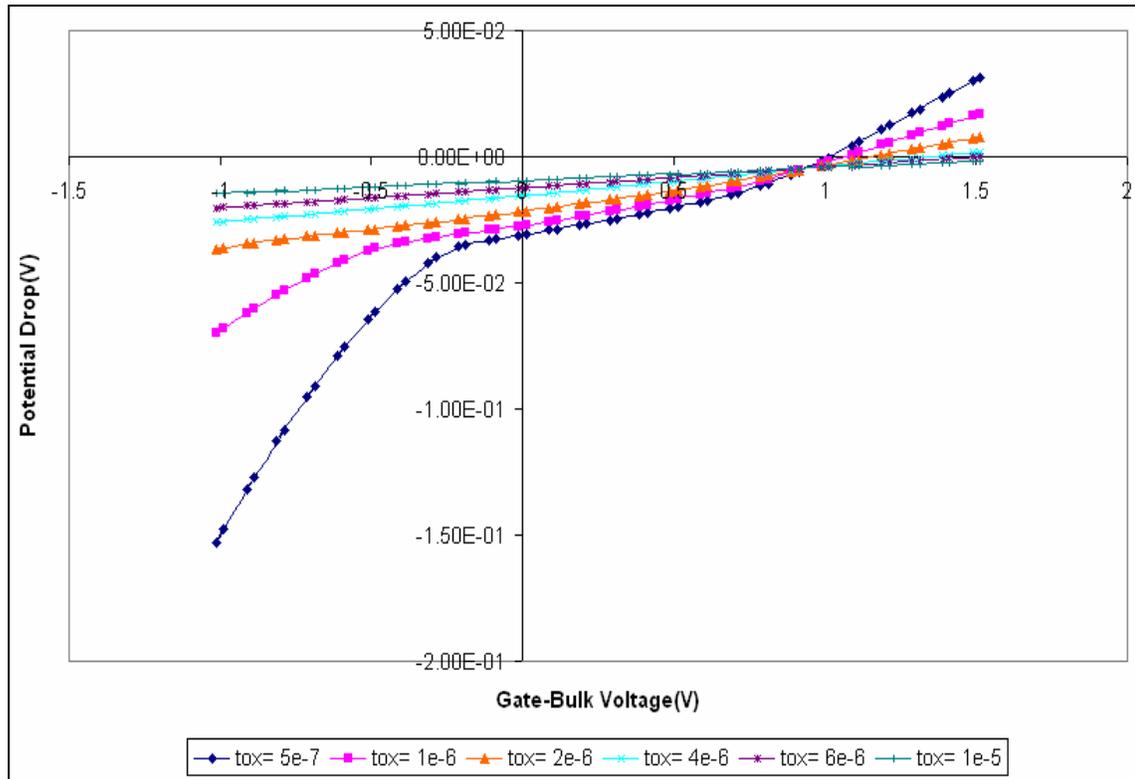


Figure 2: Potential drop vs. Gate-Bulk Voltage for various oxide thicknesses

Effect of channel length (L) on potential drop

The simulation result of the effect of the channel length on the potential drop in the gate is shown in Figure 3. It can be seen that the lateral field is decreased as the channel length is increased. The lateral field depends on the voltage between the drain and the source [8]. From the basic concept, the lateral field is proportional to the potential drop in the gate [8]. Therefore, when the lateral field is decreasing, the potential drop at the gate will be reduced. If the potential drop decreased, then the effective gate voltage will be increased and leads to the reduction in the potential drop in terms of magnitude. It can be seen that if the reference gate voltage = -0.5V is taken into consideration wider gate length produces smaller value of potential drop. Therefore when the channel length is increased, the lateral field will be decreased.

$$\Delta V_p = \frac{\Delta Q}{C_d} = \frac{2qN_d A}{LC_d} \tag{5}$$

Equation 5 implies that ΔV_p should be taken into account to reflect further polysilicon for very short gate lengths [9]. As the gate length is scaled down, the portion of the inversion capacitance decreases and potential drop increases, implying that device performance deterioration from the polysilicon depletion effect will be more significant as device is continue to scale down [9].

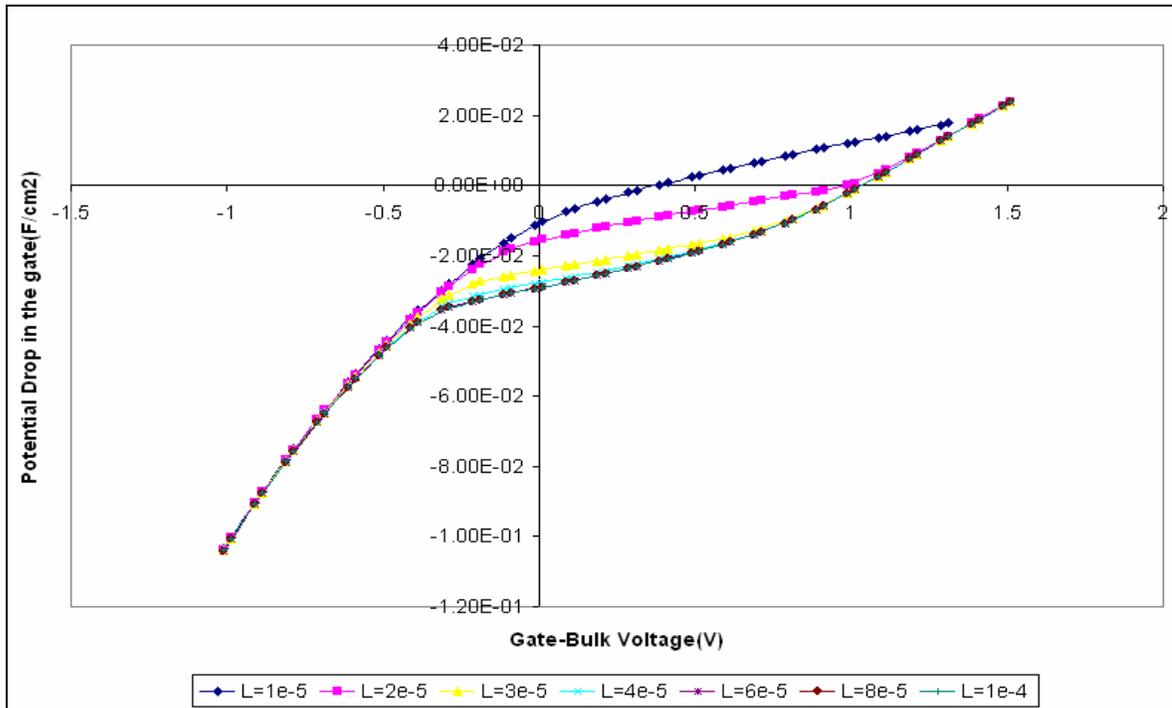


Figure 3: Potential drops vs. gate-bulk voltage for various lengths

Effect of High-K and SiO₂ dielectric with different dielectric thickness on C-V characteristics

In this analysis, polysilicon gate was used together with the SiO₂ and HfO₂ dielectric material. Based on the results (Figure 4), High-K dielectric material produces high capacitance compared to SiO₂ dielectric material even though the High-K material can prevent the leakage current flowing to the gate with higher oxide thickness as compared to SiO₂ [5]. Besides that, higher capacitance for using High-K dielectric allows good gate control and increases the drive current. The low gate currents reduce standby power dissipation for low power application. As a result, it can enhance the performance of the CMOS application.

Problem will arise when polysilicon gate is used for PPOLY/High-K dielectric stack because of High-K dielectric is incompatible due to the Fermi level pinning at the PPOLY/High-K interface which causes high threshold voltage in MOSFET transistors [10]. Fermi level pinning means that undesirable effects when a High-K dielectric gate dielectric is combined with polysilicon gate. It is difficult to adjust the threshold voltage to a low value, which is needed for high performance. It is caused by the defect formation at the PPOLY/High-K dielectric interface [9].

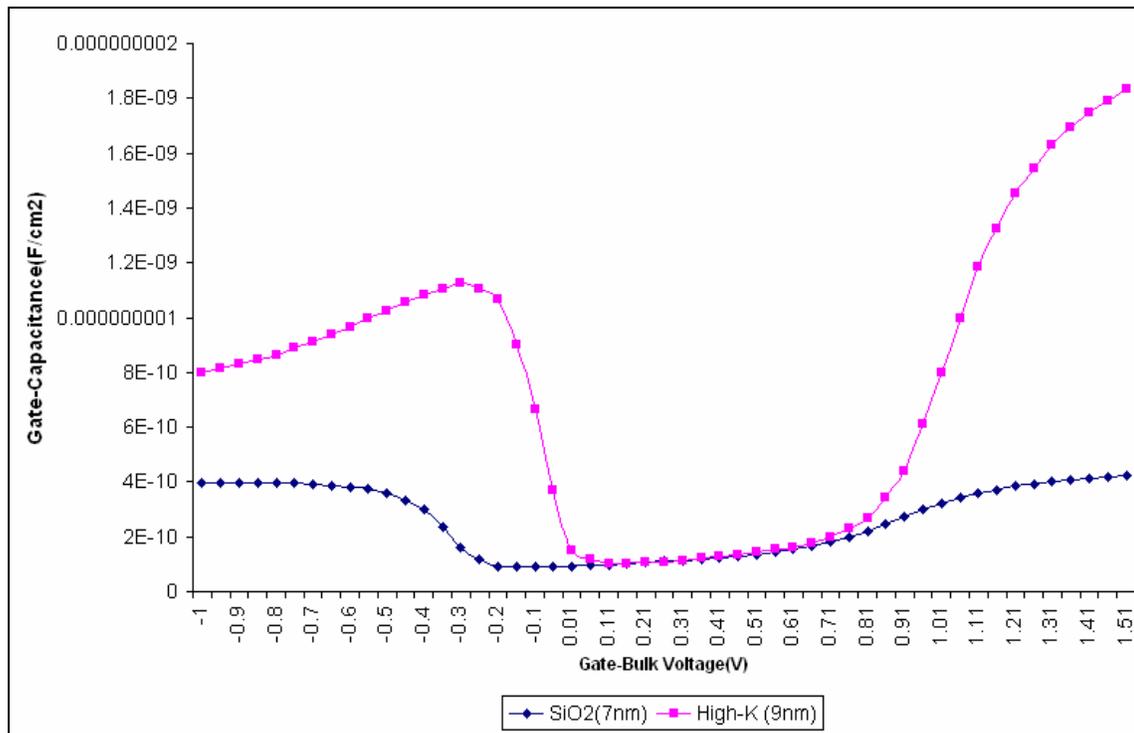


Figure 4: Graph Capacitance vs. Gate Bulk Voltage for High-K (9nm) dielectric material and SiO₂ (7nm) dielectric material.

CONCLUSION

The contribution of polysilicon gate depletion effect to the performance degradation of PMOSFETS has been proved by simulation. High-K dielectric material was found to be not compatible on polysilicon gate.

REFERENCES

- [1]. URL:<http://www.semiconductorglossary.com>
- [2]. Wong, C.Y., Sun, J.Y.C., Taur, Y., Oh, C.S., Angelucci, R. and Bavari B.(1988). "Doping of n+ and p+ Polysilicon in a Dual-Gate CMOS process." IEDM Tech.Dig." 238-241.
- [3]. Chen, K., Chan, M., Hu C., Ma, Z.J., Rabye, J.(1995). *Polysilicon depletion effect on IC performance*.
- [4]. Schuegraf, K. F., King, C. C. and Hu, C. (1993). *Int.Symp. VLSI TSA.86*.
- [5]. Ashawant G., Peng F., Miryeong S., Ming-Ren L., Don W., Kai Chen, and Chenming H. (1997). *Accurate Determination of Ultrathin Gate Oxide Thickness and Effective Polysilicon Doping of CMOS Devices*. IEEE Electron Device Letters. Vol.18 (12).
- [6]. Donald Naeman. (1997). *Semiconductor Physics & and Devices, BasicPrinsiple.2nd Edition*.MGGraw Hill,International Edition.

- [7]. Pierret, R.F. (1996). *Semiconductor Device Fundamentals*. Addison Wesley Publishing Co., Reading MA.
- [8]. Rios, R., Arora, N. D., and Huang, C.L., “An analytic polysilicon depletion effect model for MOSFETs,” *IEEE Electron Device Lett.*, vol. **15**,129–131, Apr. 1994.
- [9]. Chang, H. C., Rajesh, K.(2002), *Dopant Profile and Gate Geometric Effects on Polysilicon Gate Depletion in Scaled MOS*.*IEEE Transactions on Electron Devices*.vol.**49**(7).
- [10]. Hsueh, K. K., Sanchez, J. J., Demassa, T. A. and Akers, L. A. (1988). *Inversenarrow-width effects and small-geometry MOSFET threshold model*. *IEEE Trans. Electron Devices*. Vol. **35**.325–338.