Solid State Science and Technology, Vol. 15, No 2 (2007) 66-74
ISSN 0128-7389

IMPACT OF DELTA-DOPED POSITION ON THE PERFORMANCE OF AlGaAs/InGaAs/GaAs PSEUDOMORPHIC HIGH ELECTRON MOBILITY TRANSISTOR

Norman Fadhil Idham Muhammad, Ahmad Ismat Abdul Rahim, Rasidah Sanusi, Abdul Fatah Awang Mat and Mohamed Razman Yahya

Telekom Research &Development Sdn.Bhd., Idea Tower, UPM-MTDC Technology Incubation Center One, Lebuh Silikon, 43400 Serdang, Selangor, Malaysia

ABSTRACT

This paper reports on simulation of delta-doped AlGaAs/InGaAs/GaAs Pseudomorphic High Electron Mobility Transistors (PHEMT's) by means of two dimensional device simulations. The commercial two dimensional device simulator Taurus-MEDICI was used to study the band-diagram, threshold voltage (Vth), transconductance (G_m) and cut off frequency (f_T) of the PHEMT. Three different devices with single delta-doped layer located at three different positions in the pHEMT layer are simulated. The result shows that the position of delta-doped layer can be optimised to maximise the drain current, transconductance and cut-off frequency. It also can determine the device operation mode, whether as enhancement mode or depletion mode.

INTRODUCTION

Pseudormophic high electron mobility transistors (pHEMTs) are well kown for the use in present and emerging micro and milimeter-wave systems because of their demonstrated high speed, low noise, and good power handling capability. The advancements in epitaxial growth technology have allowed the growth of *strained* InGaAs into GaAs substrate and have enabled the construction of transistors with different bandgap than otherwise possible in conventional silicon devices. The main concern in GaAs technology is the high cost involved during the development stage. One way to reduce the number of wafers involved in the design of experiments; and hence reducing the overall development cost is to utilize commercially available Technology Computer Aided (TCAD) device simulation tools to optimize the transistor design and engineering.

In typical pHEMT device, supply layer is usually heavily doped i.e > $5x10^{17}$ cm^{-3} to obtain a high carrier sheet density to improve the supply of electrons in the channel of the transistor. However, there is a limit which the supply doping concentration can be increased as the increase in doping concentrations in the supply region, especially under the gate will cause a decrease in the gate breakdown voltage which is undesirable for power applications. One way to overcome this problem is to use an undoped supply region and to precisely control the position or location at which the doping concentration is increased (> $5X10^{17}cm^{-3}$) in the transistor i.e using the delta doping

method. This method has the benefits of increasing the sheet carrier concentration while maintaining the high breakdown voltage of the transistor [1]. Other benefits of employing delta doping are high electron mobilities, high electron saturation velocities, high current gain cut-off frequencies and low minimum noise figures [2].
So far, the delta doping method used is either a single delta doped region inside the channel or double delta doped regions both below and above the channel as depicted in figures 1(a) [3] and 1(b) [4]. In all three delta doping configurations mentioned above the electrical characteristics that are mostly affected are minimum noise figures, transconductance and cut-off frequencies.
In this work, a different delta doping configuration is used i.e by positioning the delta doping at the interface between the channel and buffer regions. For comparisons purposes delta doping is also placed in the channel region as well.

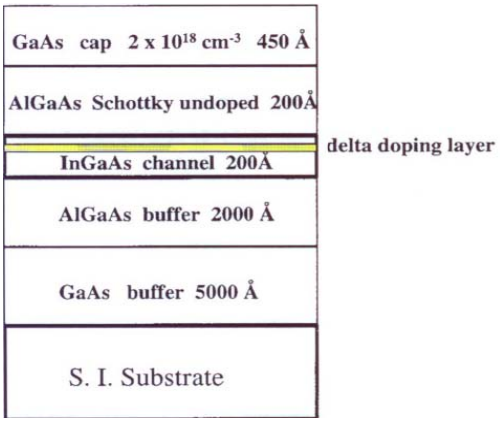

Figure 1(a): Structure with delta doping in the channel. (After Nawaz *et al*. [3])

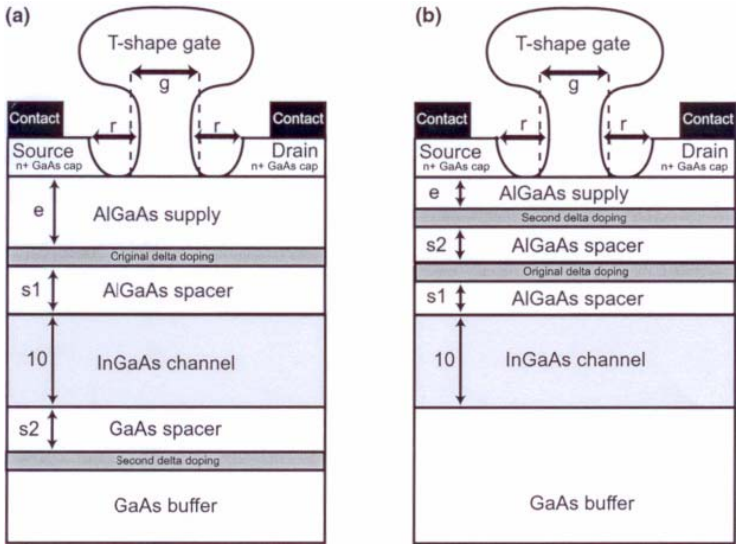

Figure 1(b): Structure with double delta doped above and below the channel. (After Kalna *et al*. [4])

Solid State Science and Technology, Vol. 15, No 2 (2007) 66-74
ISSN 0128-7389

EXPERIMENTAL PROCEDURE

The pHEMT cross section used in the simulations is shown schematically in figure 2. It consists of a 400Å of GaAs cap layer doped to 1 x 10^{20}cm^{-3}, 330Å undoped $Al_{0.2}Ga_{0.8}As$ supply layer, and 150Å undoped $In_{0.2}Ga_{0.8}As$ channel and 1μm of GaAs buffer. The gate, source and drain are surrounded with nitride which forms the passivation layer. The properties of the channel control the electron transport. The material and electrical properties change at the heterojunction interfaces i.e. at interfaces between different layers. To model the different layers correctly the PHEMT is split into different regions and the discontinuous behavior on interfaces between layers has to be treated by specific interface models to link the layers together. Shockley-Read-Hall and Auger recombination models are used to model recombination with concentration dependant lifetimes. Fermi-Dirac statistics is used to model carrier transport and the "ANALYTIC" technique is used to model concentration and temperature dependant mobilities. The source and drain contacts are placed on top of the cap layer, similar to the real device. The work function used for the Schottky gate is 5.17eV. The current-gain cut-off frequency, f_T is calculated by the approximation [5]:

$$f_T = g_m / (2C_G) \quad (1)$$

Where C_G is the total gate capacitance and g_m is the transconductance of the transistor. In this work the peak transcounductance g_m and the corresponding gate capacitance, C_G at the same V_{GS} is used to calculate f_T.

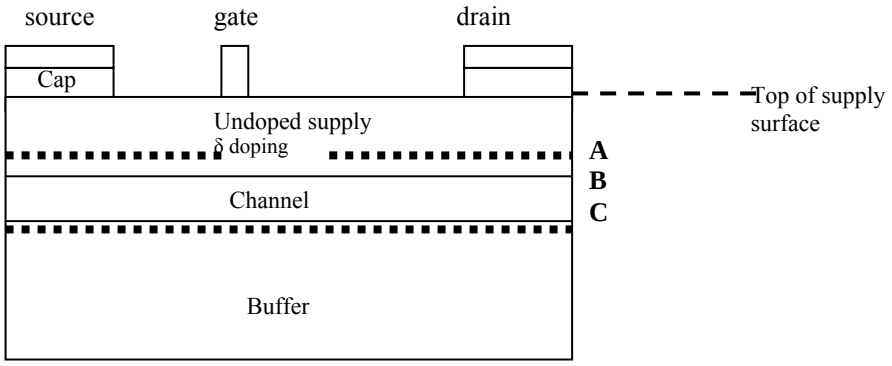

Figure 2: Schematic cross-section of the simulated PHEMT with different delta doping positions A, B and C

The delta doped region has a uniform concentration of 5X10^{19} cm $^{-3}$ and a fixed thickness of 20Å at 3 different depths i.e. 280Å (Simulation A), 310Å (Simulation B) and 370Å (Simulation C). The depths are measured from the top surface of the supply region as shown in Figure 2.

Solid State Science and Technology, Vol. 15, No 2 (2007) 66-74
ISSN 0128-7389

RESULTS AND DISCUSSION

The placing of the delta-doping at different position (A, B & C), has demonstrated different electron concentrations in the channel. At the zero bias (Figure3 (a)), curve B has the highest electron concentration ($\approx 10^{17} cm^{-3}$), curve A with electron concentration at $\approx 10^{16} cm^{-3}$ and the lowest electron concentration in the channel is curve C with $\approx 10^{12} cm^{-3}$. Figure 3(b) shows that when the transistor is biased at their repective threshold voltage (Vgs=Vth), the average electron concentration in the channel have approximately the same value i.e. $1X10^{15} cm^{-3}$ for all three cases i.e. (Simulation A, B and C). The electron concentration for Simulation B has increased at Vg=0V due to its negative threshold voltage.

Figure 4(a) and (b) showed the conduction band diagram at 0 V bias and at threshold voltage bias for each simulated device. The conduction band for Simulation B at 0V bias is located near the Fermi level and it has moved-up at threshold voltage bias. As for the simulation C, the conduction band has shifted down towards the Fermi level, at the threshold voltage bias. Meanwhile Simulation A, the conduction band has not changed either at 0V biasing or at threshold voltage. These behaviors happen due to the on state and off state for each device. For simulation B, the threshold voltage is at Vgs = -0.19V (Figure 5), therefore when the device is biased at 0V, it is in on-state which explains the conduction band near the Fermi level. The negative threshold for Simulation B is due to the presence of higher electron concentration in the channel as compared to simulation A and C. As for the simulation A and C, the on state is at bias > 0V. So the conduction band in the channel region is moving near the Fermi level when the biased is increased. Conduction band for Simulation A shows no significant different due to the threshold voltage is ≈ 0.05V which is near to 0V.

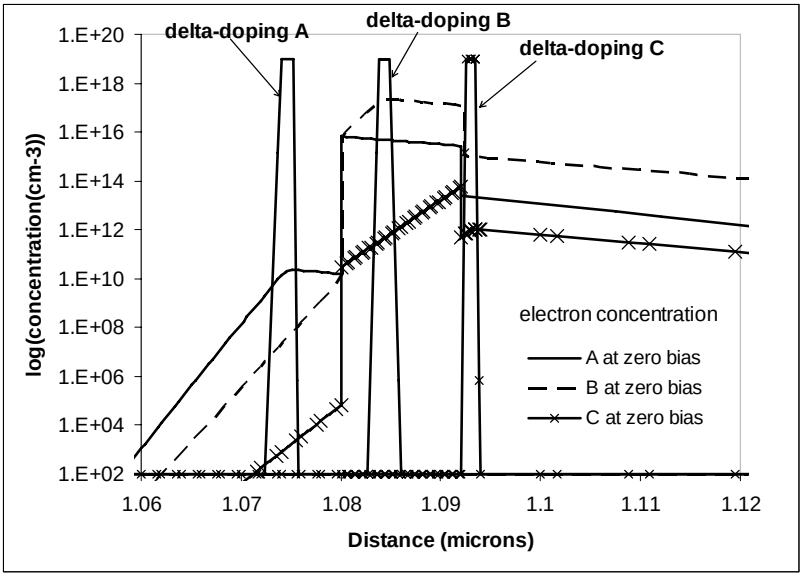

Figure 3(a): Electron and delta-doping concentration at 0V bias for each simulation

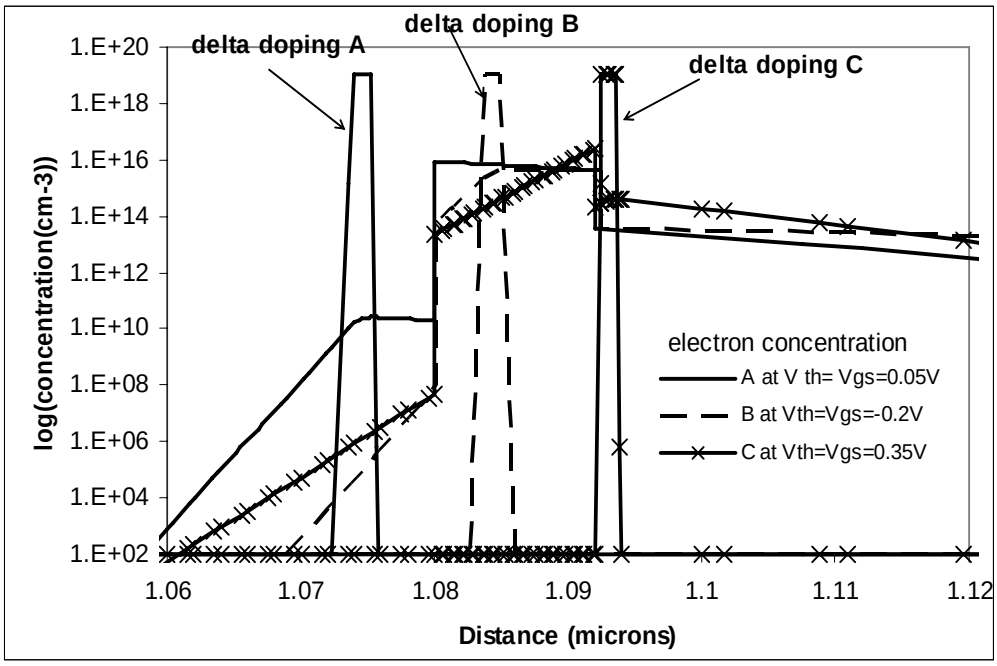

Figure 3(b): Electron and delta-doping concentration at threshold voltage, Vth, for each simulation

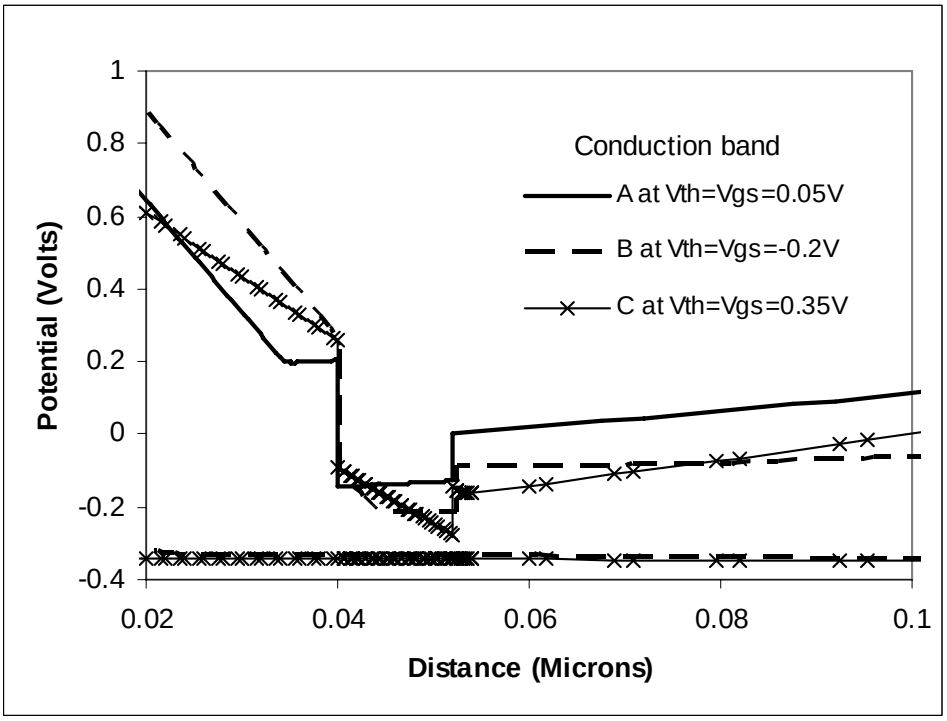

Figure 4(a): Conduction band at 0V biased

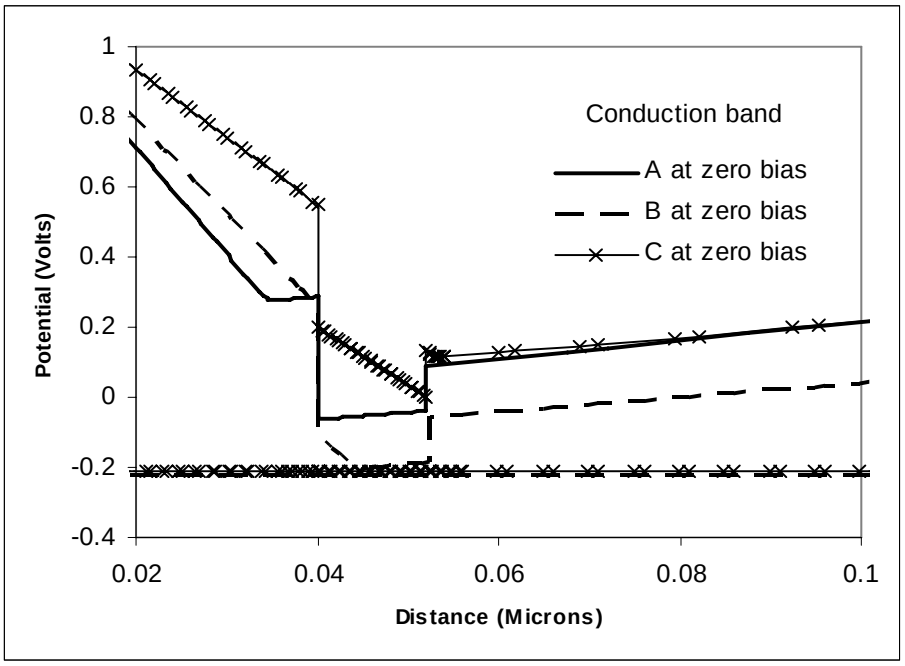

Figure 4(b): Conduction band at threshold biased

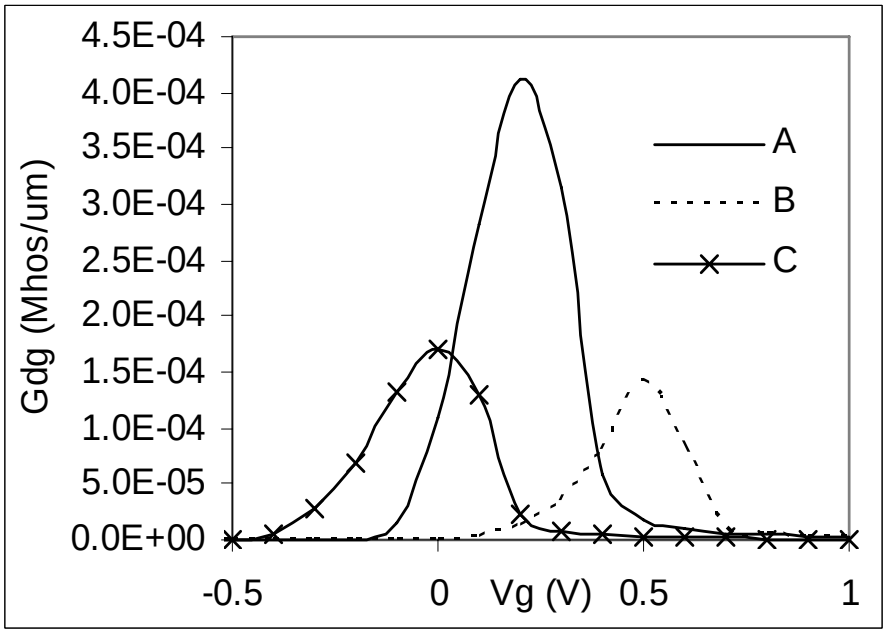

Figure 5: Ids vs Vgs for simulation A, B and C

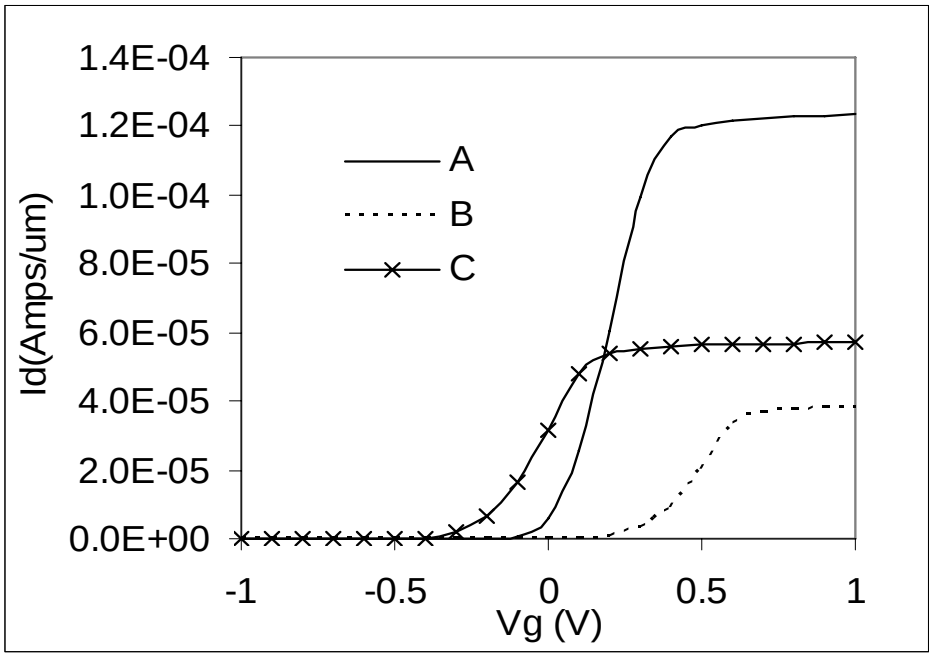

Figure 6: Transconductance, Gdg, vs gate voltage, Vgs

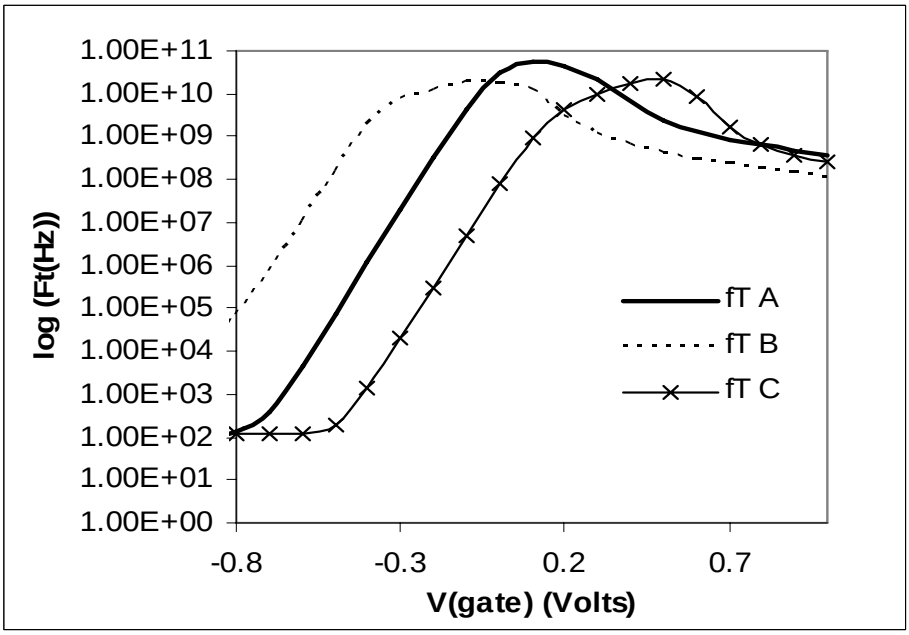

Figure 7: Gate Capacitance vs Gate Voltage for simulation A, B &C

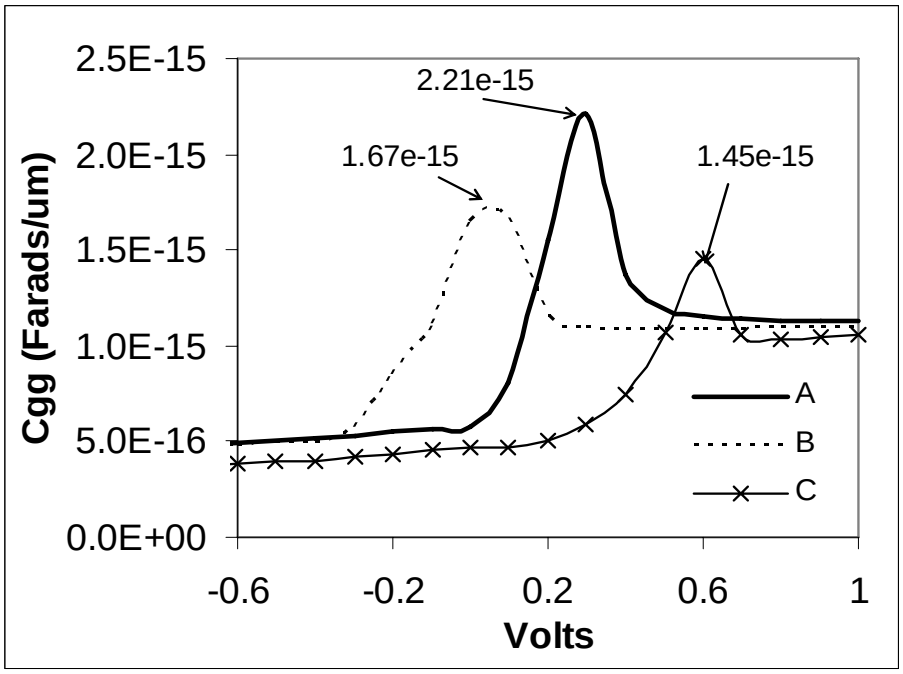

Figure 8: Cut-off frequency vs Gate Voltage for simulation A, B &C

In Figure 6, the transconductance plot against Vg shape is comparable to the IdVg plot (Figure 5). This shows that the Simulation A has the highest drain current followed by Simulation C and then Simulation B. The decreasing slope of the transconductance is caused due to the Ids saturation. As for the gate capacitance, Cgg, plot against Gate Voltage, Vgs (Figure 7), Simulation A gives the highest capacitance value. The plot is shifting accordingly to IdVg graph (Figure 5) and transconductance graph (Figure 6). Although Simulation A has demonstrated the highest gate capacitance, it still gives the highest cut-off frequency (Figure 8) at 55.6GHz. This performance is due to the high drain current and hence high transconductance for Simulation A. Simulation B gives cut- off frequency at 18.8GHz and Simulation C at 21.3 GHz.

CONCLUSION

The effect of the placements of delta-doping in the PHEMT layer has been studied using MEDICI device simulations. The position of the delta-doping layer has given a big impact to the threshold voltage and slight differences for transconductance, capacitance and cut-off frequency. The advantage of the placing delta doping layer in the PHEMT layer is one can choose whether he wants the device to be operated as enhancement mode or depletion mode device. If one wants the device to be enhancement-mode which is normally off, he can consider introducing the delta-doping above the channel or in the channel itself. As for the depletion-mode, which is the device is normally on; the delta doping layer can be placed below the channel.

ACKNOWLEDGEMENT

The authors would like to thank Telekom Malaysia Sdn. Bhd. for providing a research grant to perform the work.

REFERENCES

[1] Chang, Y. and Kuo, Y.-K. (2005); *Appl.Phys.A*, **81**, 877-879.
[2] Tian, H., Kim, K.W., Littlejohn, M.A., Bedair, S.M. and Witkowski, L.C. (1992); *IEEE Transaction on Electron Devices*, Vol. **39**, No.9.
[3] Nawaz, M. and Miranda, J.M. (2000); *Semicond. Sci. Technol*. **15**, 728-735.
[4] Kalna, K. and Asenov, A. (2004); *Solid-State Electronics*, **48**, 1223-1232.
[5] Taurus Medici-User Guide (Oct 2005), Version X-2005.10.